Applications of Magnetic Integration for Non-Isolated DC-DC Converters

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To:

My Family and Diana

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Abstract

Electric Vehicle (EV) applications are an improved, alternative and emerging technology that is causing a growing interest due to the reduced fuel consumption if offers and the benefits it brings to issues like greenhouse emissions in transportation systems. These vehicles have a long way to go in terms of technological improvements. They demand high efficient, compact and high-power converters in order to supply the enough torque and the needed speed in the daily requirements of the users. These requirements become critical especially in places with varying topography and unstable soils.

Nevertheless, high efficient, high power density and high voltage gain operation are required in the DC-DC converter that interfaces the storage unit with the electric motor and in the DC-DC converter between the storage unit and the auxiliary systems. These features allow to keep the power and autonomy of the electric propulsion system and to have an efficient use of the energy from the storage unit.

In this context, interleaving phases and magnetic integration are known as effective techniques to reduce the volume and mass of power converters as well as the probable increase of the converter efficiency. Therefore, this thesis presents a detailed analysis of several applications of magnetic integration for non-isolated DC-DC converters for these applications.

First, the total volume analysis of the two-phase interleaved boost converter with three different magnetic components is proposed. As part of this analysis, novel magnetic integration techniques and a novel technique to increase the reduce fringing losses are proposed to increase the power density and the efficiency of these converters. From this analysis, the power density is evaluated from the electric and magnetic modeling.

Second, the magnetic integration technique is evaluated in the proposed single-phase and two-phase tapped-inductor converters with saturable-inductors in order to reduce the recovery phenomenon on the main diodes. These topologies are proposed and evaluated in order to obtain a high efficiency in DC-DC conversion.

Third, for auxiliary systems where low voltage is required to feed non-propulsive load, a high step-down DC-DC converter is proposed to supply these low-voltage loads by a high voltage power supply. Therefore, a high-step-down converter with integrated winding-coupled inductor offers the advantage of a high conversion ratio keeping a high power density and a suitable efficiency. This converter is evaluated and compared with other outstanding high step-down converters.

Finally, a High Step-Up DC-DC converter is proposed as a solution for EV applications where the storage unit voltage is much lower than the voltage required by the motor. This novel converter uses the well-known technique of coupling inductors for achieving high power density and high voltage-gain. This converter is studied in detail, compare to other outstanding converters, and evaluated. Moreover, a parasitic analysis is conducted in order to evidence the advantages of the proposed converter.

In summary, the magnetic integration technique is studied and evaluated in detail for several DC-DC converter topologies, some of them proposed by the author. These analyses include electric and magnetic modeling, characterization of power devices, thermal analysis, geometry analysis, and electric and magnetic design. Moreover, all the presented analyses are validated with experimental tests and some of them with Finite Elements Modeling.

Conclusively, magnetic integration technique proved to be an effective technique with outstanding advantages that can be used in EV applications for increasing the power density, the conversion efficiency, and the voltage gain.

Keywords: DC-DC Converters; Magnetic Integration; Interleaved Converters; Coupled Inductor; Efficiency; Power Density; High Voltage Gain; Electric Vehicles.

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1. Introduction

In recent times, there has been a global concern regarding the environmental impacts of the global warming, the resources depletion, and the health problems increase related to the diseases brought by the fossil fuels burning and the greenhouse emissions [1].

In fact, 2016 has been reported as the hottest year ever with a record of 9.4°C of anomaly in certain areas of the planet versus the temperature records of the period between 1951 and 1980 [2]. This is a critical situation due to the harmful impacts that the global warming produces. The main cause of this temperature increase is the greenhouse effect. This phenomenon is produced by the accumulation of greenhouse gasses: CO2, NOx, CO, Sox, among others. Consequently, the energy that comes from the sun everyday cannot be released because of the greenhouse layer. Thereby, earth is continuously adsorbing this solar radiation and becoming heated [3].

These problems are mainly produced by the transport, energy, and heavy industries, just to give an example. These industries constitute an important source of the CO2, NOx, CO, SOx among others polluting gases [4]. In 2014, the United States reported 6.87 Gigatons of CO2 emissions. From this amount, 30% was produced by the energy generation, 26% by the transportation sector and 21% by the industry [5].

In addition, from these emissions produced by the transportation systems, 76% is generated by road transport (automobiles, trucks, etc.), 12% by air traffic, 10% by shipping, and only a 2% by rail traffic [6]. In this context, it is important to highlight the huge impact of the energy generation and transportation systems, especially the road transport, on the global warming and all its effects.

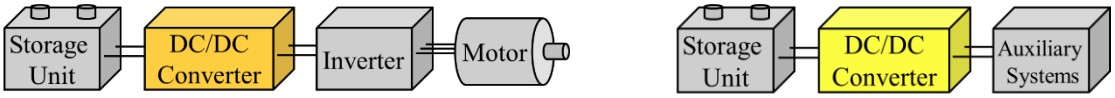
1.1 Power electronics in Renewable Energies and Electric Vehicle applications

The situation mentioned above calls for the development of renewable energies and electric transportation to contribute with solutions that help tackle these environmental issues [7]-[9]. In this context, power electronics plays a huge role because through it the efficiency of electric systems can be improved, reducing energy consumption. Especially, power converters are key subsystems in applications where power circuits interface renewable energy sources with loads, as well as energy storage units to electric motors in case of electric automotive applications (EVs applications). These applications cover the

concept of vehicles that use an electric motor for the motion of the vehicle, i.e. all the types of Hybrid Electric Vehicles (HEVs), Fuel Cell Electric Vehicles (FCEVs), and pure Electric Vehicles [10]-[16].

These automotive applications present volume and mass problems due to the following reasons: 1) EVs need heavy storage units in order to offer an acceptable autonomy to be competitive with the Internal Combustion Engine (ICE) vehicles. 2) Low efficiency electric systems produce an increase of volume and mass because additional stored energy is required to supply the power losses. And, 3) Bulky and heavy electric systems produce and excess of mass and volume because additional stored energy is needed to supply the energy to move these electric systems. To help tackle these issues, high power density DC-DC converters have attracted considerable attention in the last years [17]-[23].

Consequently, downsizing of the electric powertrains in EV applications becomes essential to increase their performance. Specifically, if the DC-DC converter that interfaces the storage unit with the electric motor is downsized, the energy from the storage devices will be better used because the vehicle systems will be lighter and smaller [24]-[27]. Figure 1.1(a) shows the electric power train of several EV applications where a step-up DC-DC converter is used to boost the voltage of the storage unit in order to achieve the voltage of the motor. Figure 1.1(b) shows the electrical system needed to feed the auxiliary systems, where a step-down DC-DC converter is required.



(a) Electric power train (b) Auxiliary systems

Figure 1.1. Electric systems in EV applications.

1.2 Isolated and Non-Isolated converters

There are two types of DC-DC converters: Isolated and Non-Isolated. The main difference between these two types is the dielectric isolation between the input and the output networks. In other words, isolated converters do not present an electric contact between the input and the output circuits. Isolated converters offer the advantages of 1) in the absence of electric contact, a safety condition is produced for both the input and the output circuit, as well as for the personnel or the circuit user. This condition is presented because three will not be an electric current transmission in case of a circuit failure; 2) Following the previous concept, the isolation between the circuits also prevents the transmission to the output of voltage transients produced in the input side. This transmission absence generated a great blocking capability of noise and interferences: and, 3) Isolated converters can offer different grounding configurations: Negative or positive ground, or even floating ground. Therefore, these converters can be configured to provide negative or positive voltages depending on the load. Isolated converters are widely used in communications where loads are highly sensitive [28]-[30].

Nevertheless, isolated converters present drawbacks of big size. Usually, these converters use bulky transformers and more components that non-isolated converters. Thus, volume, mass, cost, and power losses in some cases of isolated converters are bigger than the case of non-isolated converters.

Non-isolated DC-DC converters offer the advantages of lower cost, and high power density. Consequently, in applications of electric mobility where the DC-DC converters of Figure 1.1 are not continuously connected to the grid, non-isolated converters are suitable candidates to be installed in these applications [31].

1.3 Multi-phase and magnetic integration in Non-Isolated converters

EV applications have conventionally used non-isolated converter topologies like the well-known single-phase boost converter. Figure 1.2 shows the schematic of a single-phase boost converter [32]-[37]. This topology presents some drawbacks that may decrease the vehicle performance. Among those are recognized: 1) switches and diodes are operated under hard switching which produce EMI/RFI noises and large switching losses; 2) Large conduction losses in the windings and in the power devices are produced by the large peak current generated when the voltage of the storage unit is quite lower than the output voltage. This behavior results from the high duty cycle produced to obtain a high voltage-gain; and 3) large mass and volume of the cooling system due to additional components employed for dissipating power losses. Consequently, novel techniques, that offer reduction of mass and volume as well as efficiency increase, are required for these EV applications.

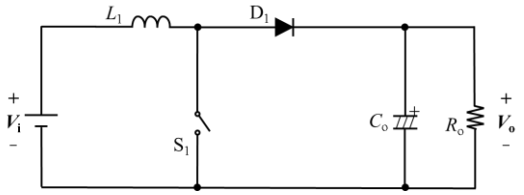


Figure 1.2. Single-phase boost converter.

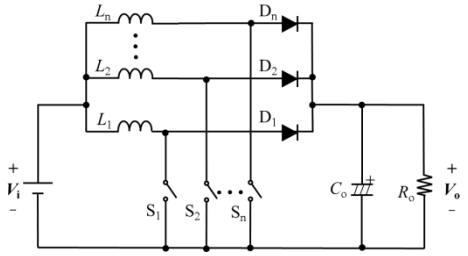


Figure 1.3. Interleaved boost converter.

Consequently, interleaving phases and magnetic coupling are studied in this document in order to offer solutions to the problems described before. Interleaving-phases is an effective technique because it offers the following advantages: 1) input current is divided into the number of phases. Therefore, a reduction in the power ratings of the components is generated, and this may cause a reduction of the power losses and therefore a heat sink volume reduction; 2) a size miniaturization of the capacitive components results from the high frequency operation produced by the power transmission alternation in each phase; 3) Electromagnetic Interference (EMI) suppression is presented when the number of phases in interleaved converters is increased or when the phase shift is changed.

Figure 1.3 shows the schematic of an interleaved boost converter with n-phases. Nevertheless, interleaving technique presents the disadvantage of increasing the volume and weight of the magnetic components because each phase needs its own inductor [38]-[42].

In this context, magnetic coupling is introduced as an effective technique because: 1) DC fluxes generated by DC currents can be effectively canceled when an inversely coupling is used. In addition, the AC flux may be reduced in certain parts of the core. Therefore, a size reduction of the magnetic components may result from the integration of several windings into only one core. 2) Inductor current ripples in each phase can be reduced due to the mutual effect. As a result, smaller inductances in each phase can be used for realizing the same inductor ripple currents of non-coupled inductors. 3) Transient response speed is improved because the inductor current rate becomes higher than the one of the non-coupled inductor [43]-[49].

1.4 Outline of the thesis

This document presents the volume analysis of outstanding two-phase DC-DC converters. In addition, it proposes four topologies of DC-DC converters using the techniques of interleaving phases and magnetic coupling. Chapter 2 presents a review of the two-phase interleaved boost converter with coupled-inductors. Volume and efficiency trends are studied and evaluated. Chapter 3 proposes a single-phase and a two-phase DC-DC converter for reducing the recovery losses on the power diodes. These converters offer the novelty of the inclusion of saturable inductors with the purpose of reducing the slope of the diode current and thereby the reverse recovery reduction. Chapters 4 and 5 present the application of magnetic integration and interleaving phases for obtaining high voltage-gains. As it was explained above, conventional converters often present some problems when a high voltage-gain is required to produce it, a large duty cycle and large currents are needed. These conditions increase the conduction losses especially caused by the parasitic components, and in most cases a high voltage-gain is not reached because of these losses. Consequently. Chapter 4 derives a method for achieving a high step-down ratio in a converter aimed to be applied for low voltage systems in EV applications (Figure 1.1 (b)) or in renewable energy applications. Chapter 5 proposes a high voltage-gain converter using the technique of chapter 4. In chapters 4 and 5, the study of the high voltage-gain converters is conducted through the steady state analysis, comparison with outstanding converters reported in the literature, and the analysis of the effect of parasitic components on the voltage gain. Finally, conclusions are given to this document as well as the list of publications resulting of this research.

References

[1] IARC – International Agency for Research on Cancer, "Diesel Engine Exhaust Carcinogenic," *World Health Organization*. pp. 1-4. 2012.

[2] GISS Surface Temperature Analysis (GISTEMP) Retrieved from http://data.giss.nasa.gov/gistemp/.

[3] C. Gibbs, and M. Cassidy, "2 Crimes in the carbon market," Handbook of Transnational Environmental Crime, 235. 2016.

[4] UNFCC –United Nations Framework Convention on Climate Change. "National greenhouse gas inventories," *Unfccc Resource Guide*. p. 31. 2010.

[5] EPA – US Environmental Protection Agency, "U.S. Greenhouse Gas Inventory Report: 1990-2014," Retrieved from https://www3.epa.gov/climatechange/ghgemissions/usinventoryreport.html

[6] IEA-International Energy Agency, "Energy and Climate Change," *World Energy Outlook Special Report,* 2015.

[7] J. Dixon, M. Ortuzar, and E. Wiechmann, "Regenerative Braking for an Electric Vehicle Using Ultracapacitors and a Buck-Boost Converter" Catholic University of Chile. pp. 1-4. 2008.

[8] C. Bonfiglio and W. Roessler, "A Cost Optimized Battery Management System with Active Cell Balancing for Lithium Ion Battery Stacks", Vehicle Power and Propulsion Conference, VPPC '09, pp. 304 - 309. 2009.

[9] C. Shumei, L. Chen and S Liwei, "Study on efficiency calculation model of induction motors for electric vehicle", IEEE Vehicle Power and Propulsion Conference, VPPC '08, pp. 1-5. 2008.

[10] I. Aharon and A. Kuperman, "Topological Overview of Powertrains for Battery-Powered Vehicles with Range Extenders" IEEE transactions on power electronics, Vol 26, no. 3, pp. 867 -870. 2011.

[11] A. Burke, "Batteries and Ultracapacitors for Electric, Hybrid, and Fuel Cell Vehicles", Proceedings of the IEEE, Vol 95, pp. 808 - 811. 2007.

[12] A. Burke, "Ultracapacitors: why, how, and where is the technology", Journal of power sources, vol. 91, pp. 37-50, 2000.

[13] J. Dixon, I. Nakashima, E. Arcos and M. Artuzar, "Electric vehicle using a combination of ultracapacitors and zebra battery", IEEE transactions on industrial electronics, Vol 57, pp. 943 - 947. 2010.

[14] T. Gillespie, "Fundamentals of vehicle dynamics", 1st Ed., SAE International, 1992.

[15] P. Bossche, F. Vergels, J. Mierlo, J, Matheys and W. Autenboer, "SUBAT: An assessment of sustainable battery technology", Journal of Power Sources (2005), Vol 162. Pp. 913-919. 2005.

[16] International Energy Agency – IEA, "Technology Roadmap Electric and plug-in hybrid electric vehicles (EV/PHEV)", pp. 10 - 14. 2011.

[17] H. Zhai, "Comparison of Flexible Fuel Vehicle and Life-Cycle Fuel Consumption and Emissions of Selected Pollutants and Greenhouse Gases for Ethanol 85 Versus Gasoline," *Journal of the Air & Waste Management Association*, Vol. 59 no. 8, pp. 912-24. 2009.

[18] R. Kemp et al., Electric Vehicles: Charged with Potential. London, U.K.: Royal Academy of Engineering, 2010.

[19] S. Peeta and A. K. Ziliaskopoulos, "Foundations of dynamic traffic assignment: The past, the present and the future," *Netw. Spatial Econ.*, vol. 1, no. 3/4, pp. 233–265, Sep. 2001.

[20] W. Martinez, C. Cortes and L. Munoz, "Sizing of Ultracapacitors and Batteries for a High Performance Electric Vehicle," *IEEE International Electric Vehicle Conference (IEVC),* pp. 535-541. 2012.

[21] IEA, Energy Technology Perspectives, scenarios & strategies to 2050 by International Energy Agency, 2010.

[22] J. Bishop, et al., "Investigating the technical, economic and environmental performance of electric vehicles in the real-world: A case study using electric scooters," *Journal of Power Sources*, Vol. 196, pp. 10094–10104. 2011.

[23] P. Baptista, M. Tomas, C. Silva, "Plug-in hybrid fuel cell vehicles market penetration scenarios," *International Journal of Hydrogen Energy*, Vol. 35 no. 18, pp. 10024- 10030. 2010.

[24] Y. Cheng, R. Trigui, C. Espanet, A. Bouscayrol, and S. Cui, "Specifications and Design of a PM Electric Variable Transmission for Toyota Prius II," *IEEE Trans. on Vehicular Technology*, vol. 60, no.9, pp.4106-4114, Nov. 2011.

[25] M. Pavlovsky, Y. Tsuruta, A. Kawamura, "Recent improvements of efficiency and power density of DC-DC converters for automotive applications", The 2010 International Power Electronics Conference (IPEC), pp.1866-1873, 2010.

[26] C. Chan, A. Bouscayrol, K. Chen, "Electric, Hybrid, and Fuel-Cell Vehicles: Architectures and Modeling", IEEE Transactions on Veh. Technol., vol. 59, no. 2, pp. 589-598, 2010.

[27] M. Yilmaz and P. Krein, "Review of Battery Charger Topologies, Charging Power Levels, and Infrastructure for Plug-In Electric and Hybrid Vehicles," *IEEE Trans. on Power Electronics,* vol. 28, no. 5, pp. 2151-2169, May. 2013.

[28] H. Mao, L. Yao, J. Liu, and I. Batarseh, "Comparison study of inductors current sharing in non-isolated and isolated DC-DC converters with interleaved structures,". *31st Annual Conference of IEEE Industrial Electronics Society, IECON* pp. 1-7, 2005.

[29] M. Prudente, L. Pfitscher, G. Emmendoerfer, E. Romaneli, and R. Gules, R. "Voltage multiplier cells applied to non-isolated DC–DC converters," *IEEE Transactions on Power Electronics*, 23(2), 871-887. 2008.

[30] Y. Du, X. Zhou, S. Bai, S. Lukic, and A. Huang, "Review of non-isolated bi-directional DC-DC converters for plug-in hybrid electric vehicle charge station application at municipal parking decks," *Applied Power Electronics Conference and Exposition (APEC),* pp. 1145-1151. 2008.

[31] W. Li, X. Lv, Y. Deng, J. Liu, and X. He, "A review of non-isolated high step-up DC/DC converters in renewable energy applications," *Applied Power Electronics Conference and Exposition, APEC*, pp. 364-369, 2009.

[32] F. Guedon, S. Singh, R. McMahon and F. Udrea, "Boost Converter with SiC JFETs: Comparison with CoolMOS and Tests at Elevated Case Temperature," *IEEE Transactions on Power Electronics*, vol.28, no.4, pp.1938-1945, 2013.

[33] Toyota Motor Corporation, "Toyota Prius V Hybrid Vehicle Dismantling Manual", pp. 1-30, 2011.

[34] W. Li and X. He, "ZVT interleaved boost converters for high-efficiency, high step-up DC-DC conversion," *IET Trans. Power Electron.*, vol. 1, no. 2, pp. 284–290, 2007.

[35] R. Wai, C. Lin, R. Duan and Y. Chang, "High-efficiency DC–DC converter with high voltage gain and reduced switch stress", IEEE Trans. Ind. Electron., vol. 54, no. 1, pp. 354–364, 2007.

[36] R. Erickson and D. Maksimovic: "Fundamentals of Power Electronics", 2nd ed. Norwell, MA: Kluwer, 2001.

[37] Y. Zhao; W. Li and X. He: "Single-Phase Improved Active Clamp Coupled-Inductor-Based Converter with Extended Voltage Doubler Cell" IEEE Transactions on Power Electronics, vol.27, no.6, pp.2869,2878, 2012.

[38] K. Katsura and M. Yamamoto, "Optimal stability control method for transformer-linked three-phase boost chopper circuit," *IEEE Energy Conversion Congress and Exposition (ECCE),* pp. 1082–1087. 2012.

[39] L. Tang and G. Su, "An Interleaved Reduced-Component-Count Multivoltage Bus DC/DC Converter for Fuel Cell Powered Electric Vehicle Applications", *IEEE Trans. on Industry Applications*, vol. 44, no. 5, pp. 1638-1644, Sep. 2008.

[40] F. Yang, X. Ruan, Y. Yang, Z. Ye, "Interleaved Critical Current Mode Boost PFC Converter with Coupled Inductor," *IEEE Trans. Power Electron.*, vol.26, no. 9, pp. 2404-2413, 2011.

[41] J. Gu, J. Lai, N. Kees, and C. Zheng, "Hybrid-Switching Full-Bridge DC–DC Converter with Minimal Voltage Stress of Bridge Rectifier, Reduced Circulating Losses, and Filter Requirement for Electric Vehicle Battery Chargers," *IEEE Trans. on Power Electronics*, vol. 28, no.3, pp.1132-1144, Mar. 2013.

[42] U. Sebastian, P, Johannes, "Current-balancing Controller Requirements of Automotive Multi-Phase Converters with Coupled Inductors", *Proc. IEEE Energy Conver. Cong. Expo. (ECCE)*, pp. 372-379, 2012.

[43] S. Kimura, J. Imaoka and M. Yamamoto, "Potential power analysis and evaluation for interleaved boost converter with close-coupled inductor", *IEEE 10th International Conference on Power Electronics and Drive Systems (PEDS)*, pp.26-31, 2013.

[44] Y. Suh, T. Kang, H. Park, B. Kang and S. Kim, "Bi-directional Power Flow Rapid Charging System Using Coupled Inductor for Electric Vehicle", *IEEE Energy Conversion Congress and Expo (ECCE2012)*, pp. 3387-3394, 2010.

[45] M. Hirakawa, Y. Watanabe, M. Nagano, K. Andoh, S. Nakatomi, S. Hashino and T. Shimizu, "High Power DC/DC Converter using Extreme Close-Coupled Inductors aimed for Electric Vehicles", *Proc. the 2010 international Power Electron. Conf. (ECCE ASIA 2010)*, pp.2941-2948 ,2010

[46] K. J. Hartnett, J. G. Hayes, M. G. Egan, M. S. Rylko, "CCTT-Core Split-Winding Integrated Magnetic for High-power DC-DC Converters", *IEEE Trans. Power Electron*, Vol.28. pp. 4970-4984, 2013.

[47] J. Imaoka, Y. Ishikura, T. Kawashima, M. Yamamoto, "Optimal Design Method for Interleaved Single-phase PFC Converter with Coupled Inductor", *IEEE Energy Conversion Congress and Expo (ECCE2011)*, pp. 1807-1812, 2011.

[48] J. C. Schroeder and F. W. Fuchs, "Detailed Characterization of Coupled Inductors in Interleaved Converters Regarding the Demand for Additional Filtering", *Proc. IEEE Energy Conver. Cong. and Expo. (ECCE)*, pp.759-766, 2012.

[49] M. Pavlovsky, G. Guidi and A. Kawamura, "Assessment of Coupled and Independent Phase Designs of Interleaved Multiphase Buck/Boost DC–DC Converter for EV Power Train," *IEEE Trans. on Power Electronics*, vol. 29, no.6, pp. 2693-2704, Jun. 2014.

2. Two-Phase Interleaved Boost Converter

2.1 Introduction

Many converter topologies reported as effective for electric mobility applications have been proposed [1],[2],[4], [7]-[17]. Each topology offers different advantages for the vehicle performance. However, in order to evaluate the power density characteristics of these topologies, a volume comparison is required. Thereby, based on this characterization a design criterion to downsize the electric power train of the vehicle is proposed.

This chapter presents the electric and magnetic analysis of inductor arrangements using the magnetic coupling technique to the two-phase interleaved boost converter. These topologies appear as promising candidates to be applied in EV applications. Specifically, the studied arrangements are the topologies with Loosely Coupled-Inductor (LCI) and Closed Coupled-Inductor (CCI). In addition, in this chapter the recently proposed arrangement of the Integrated Winding Coupled-Inductor (IWCI) is also reviewed. Figure 2.1 shows the schematics of these three magnetic components.

It is important to mention that CCI is divided into a single winding inductor and a transformer achieving higher filtering because of the sum of two magnetic components. In addition, in the CCI converter, different core materials can be selected for the inductor and the transformer, e.g. the single inductor can be made of high flux density materials (Amorphous, Nanocrystaline, Powder, etc.) while the transformer can use Ferrites [16]. However, the CCI evaluation and comparison is not conducted because the interleaved circuit with LCI integrates the concept of inductor and transformer of the CCI converter into only one core resulting in a direct reduction of the number of magnetic cores. Therefore, the LCI is evaluated instead of the CCI.

Additionally, the conventional single-phase boost converter with only one magnetic component, and the two-phase interleaved boost converter with non-coupled inductors (two magnetic components) are evaluated with the purpose of showing the outstanding advantages of the interleaving phases and the magnetic coupling techniques.

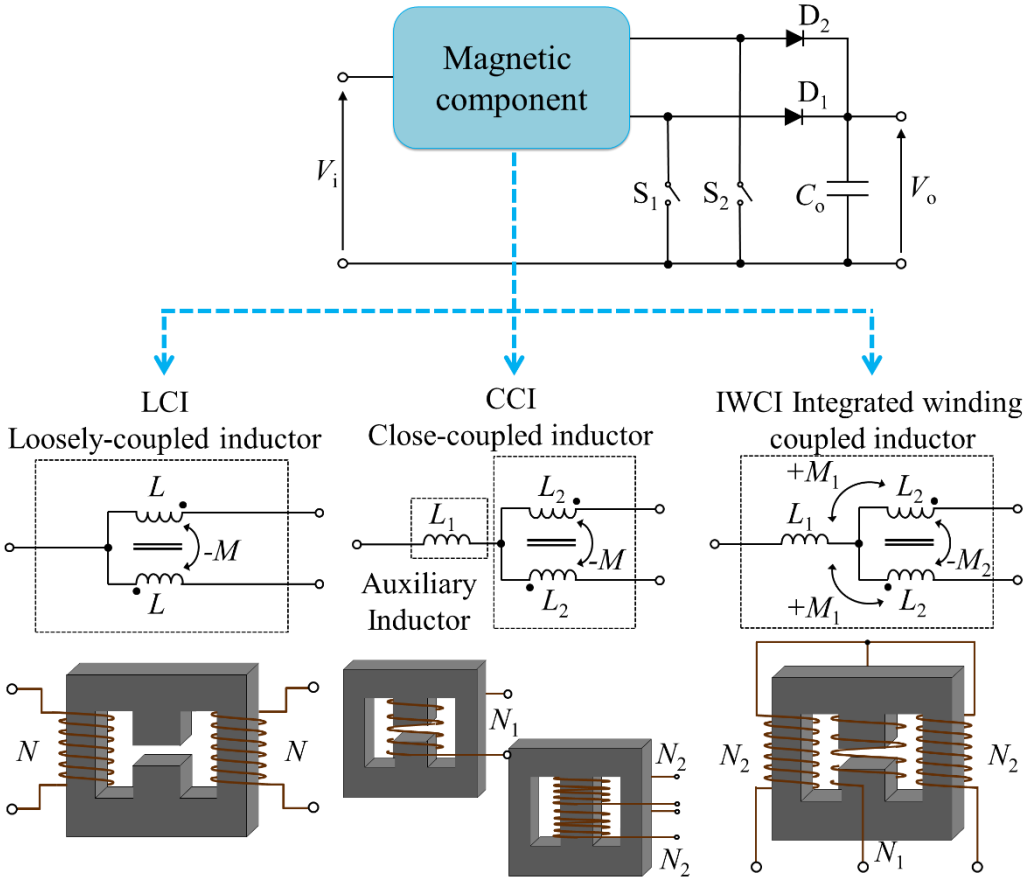


Figure 2.1. Interleaved boost converter with integrated magnetic components: LCI, CCI and IWCI

In Figure 2.1, L corresponds to the self-inductances; M are the mutual inductances between the windings; and $N$are the number of turns of each winding. In addition, in order to evaluate the magnetic coupling technique, the two-phase interleaved boost converter with non-coupled inductors is considered as well.

These topologies were selected because the interleaving-phases technique is expected to downsize the output capacitor, as a higher frequency is achieved by power transmission alternation in each phase [20]. In addition, the magnetic coupling technique is effective because the inductor current ripple presents a higher frequency behavior, and DC fluxes can be cancelled due to the mutual induction effect [15].

The analysis is conducted in several steps: 1) Geometry sizing of each magnetic component is calculated considering the inductor model; 2) Power losses of each magnetic component are calculated with the purpose of obtaining the efficiency of each inductor; 3) Semiconductor power loss calculation is carried out for sizing the required cooling device needed to dissipate these losses; 4) Finally, the total volume of each converter is evaluated and compared. As an evaluation example, the volume and the power loss analyses are conducted on four converters having the parameters shown in Table 2.1.

The parameters of Table I were selected as a model of the DC-DC converter of the Toyota Prius III. This scale model is set as 1/60 of the power of the Prius' converter and it was chosen due to the available equipment for tests and safety conditions. This case study will suggest the qualitative advantages and disadvantages of the four topologies by the volume evaluation of their entire structure.

Table 2.1.Converter Parameters for Two-Phase Converter Evaluation

Parameters	Value
Input Voltage [V]	80
Output Voltage [V]	200
Power [kW]	1
Switching Frequency [kHz]	50
Duty Cycle	0.6
Input Ripple Current [%]	20
Output Ripple Voltage [%]	0.1

2.2 Inductor Sizing

In order to conduct the volume evaluation of the selected topologies, inductor volume sizing and loss calculations are required. Thus, the definition of the core and winding geometries is presented as the base of the volume and power loss analysis. In this section, the size of each inductor is analyzed considering a Continuous Current Mode (CCM) condition. This is because magnetic components are usually designed at maximum ratings, and Discontinuous Current Mode (DCM) is not effective in high power applications because conduction losses tend to increase.

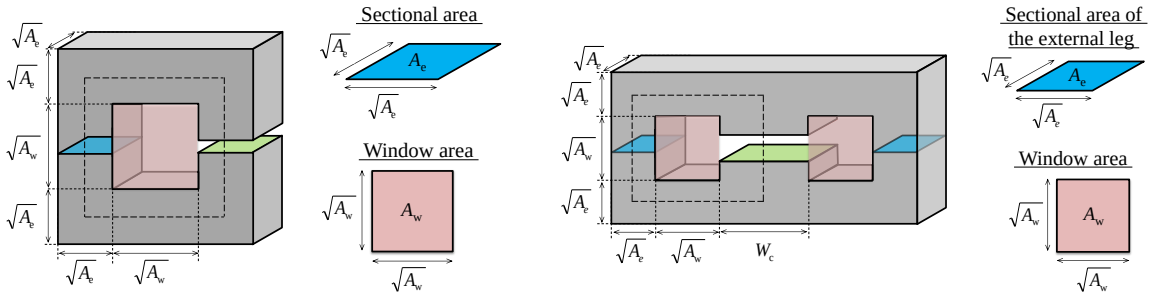
2.2.1 Core size

Volume analysis of the inductors of each topology is carried out based on the core modeling with the geometries presented in Figure 2.2. Usually, non-coupled inductors can use two-leg cores (conventionally CC, CI or U cores) or in some cases three-leg cores. Figure 2.2(a) shows the dimensions of the geometry for non-coupled inductors, and, Figure 2.2(b) shows the geometry dimensions for the three-leg cores (usually EE, EI, EC or EER cores) used by the LCI and IWCI converter. These types of geometries employ a central leg because of the increasing of the leakage inductance.

With the purpose of simplifying the calculation of the dimensions and thereby the volume of the core, most of the dimensions are set according to the sectional area of the core A_e. Moreover, the sectional areas and the window areas are assumed as squares for convenience in the calculation.

The selected core material for this evaluation example is a TDK ferrite of reference PC40, with a saturation flux density of 380mT at 100°C, a remanent flux density of 125mT,

and a relative permeability of 2300. Consequently, for these analyses, we set a maximum flux density of 250mT.



(a) Core geometry for Single-Phase and Interleaved converters

(b) Core geometry for LCI and IWCI converters

Figure 2.2. Core geometries.

2.2.2 Core losses

Core losses are mainly dependent on the eddy currents and the hysteresis process, and can be calculated by the well-known Steinmetz Equation (SE) [20]-[23]. However, this calculation method is limited because it is valid only under a sinusoidal excitation condition. For this problem, the improved Generalized Steinmetz Equation (iGSE) was proposed [21]. In this context, using the SE parameters of the PC40 material, the core losses can be calculated as follows:

$$P_{cv} = \frac{1}{T_{sw}} \int_0^{T_{sw}} k_i \cdot \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{2.1}$$

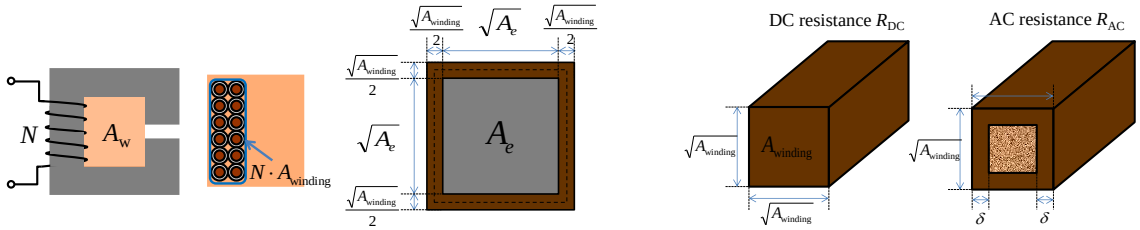
$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{2.2}$$

where dB/dt is the slope of the flux density; ΔB is the peak-to-peak flux density; T_{sw} is the switching period; and V_c is the volume of the core. k, α, ß are the Steinmetz parameters obtained from the datasheets of the PC40 core material. In the example case, k=4.5×10-14, α=1.55, and β=2.5. k_i can be calculated by applying these parameters to equation (2.2), and core losses per volume is obtained from (2.1) [20],[24].

2.2.3 Winding size

Winding volume is calculated to complete the total inductor volume. This analysis is conducted on the base of the winding geometry illustrated in Figure 2.3(a). As well as the core geometry description, winding geometry was set as squared for convenience in the

calculation. In addition, the winding volume is calculated in accordance with the sectional area of the surrounded core, see Figure 2.2 and Figure 2.3.



(a) Winding geometry (b) Winding resistances geometry

Figure 2.3. Winding geometries.

2.2.4 Winding losses

Finally, the calculation of the winding losses is needed to complete the inductor efficiency analysis. These losses are generated by the DC resistance of the total winding and the AC resistance affected by the skin-effect. Figure 2.3(b) shows the geometry of each resistance. Winding losses are derived as follows:

$$P_{winding} = R_{DC} I_L^{\,2} + R_{AC} \Delta I_{Lrms}^{\,2} \tag{2.3}$$

where R_{DC} and R_{AC} are the DC and AC (at high frequency) resistance respectively, I_L is the DC component of the inductor current, and ΔI_{Lrms} is the effective value of the inductor current ripple. In this context, DC resistance is dependent on the length of the winding, the sectional area of the wire and the wire material. In addition, AC resistance, where the skin effect is considered, can be calculated as:

$$R_{AC} = \rho \cdot \frac{l}{\pi\left(\frac{d}{2}\right)^2 - \pi\left(\frac{d}{2} - \delta\right)^2} = \rho \cdot \frac{l}{\pi\delta(d-\delta)} \tag{2.4}$$

$$\delta = \sqrt{\frac{\rho}{\pi \mu_0 f_{sw}}} \tag{2.5}$$

where ρ is the resistivity of the winding materials, d is the diameter of the wire, l is the winding length, δ is the skin depth, and μ_0 is the permeability of the free space.

2.3 Inductor Modeling

After the definition of each geometry that affects the power density and the efficiency of the inductor in the selected topologies, the inductor modeling is conducted. Therefore, regarding the volume comparison, regarding the volume comparison, the behavior of the

magnetic flux that flows in each magnetic component of the four converters is analyzed. The maximum flux intensity is defined as:

$$\phi_{\max} = \phi_{DC} + \frac{\phi_{AC}}{2} \tag{2.6}$$

where Φ_{DC} and Φ_{AC} are the average and the peak-to-peak magnetic fluxes in the core. The derivation of the maximum flux in each of the four topologies is presented in [11]-[19].

The required sectional area can be calculated with the derived magnetic flux of each topology and the maximum magnetic flux density of the selected material ($A_e = \Phi_{max} / B_{max}$). In the case of the four topologies evaluated in this study, their maximum magnetic flux density has been previously derived and presented in [12]-[19].

2.3.1 Single phase converter

The single-phase boost converter has only one inductor with one winding of N turns. Based on the overall modeling presented in [24], it is possible to derive the sectional area calculation as follows:

$$A_e = \frac{1}{B_{\max}} \left[\frac{(I_L + \frac{\Delta I_L}{2}) V_{\text{in}} D}{\Delta I_L N f_{sw}} \right] \tag{2.7}$$

where ΔI_L is the ripple current through the inductor, V_{in} is the input voltage, and D is the duty cycle.

2.3.2 Interleaved converter with non-coupled inductors

Figure 2.1 shows the two-phase interleaved boost converter with non-coupled inductors. Each inductor has one winding of N turns. Consequently, as it is reported in many studies [12]-[13], the operating principle of this topology is the same as the conventional single-phase boost converter with the exception of the phase-shift in the switching process of the switches. Therefore, the sectional area calculation according to the magnetic flux is modeled as follows:

$$A_e = \frac{1}{B_{\max}} \left[\frac{(2 I_{ph} + \Delta I_L) V_{in} D}{2 \Delta I_L N f_{sw}} \right] \tag{2.8}$$

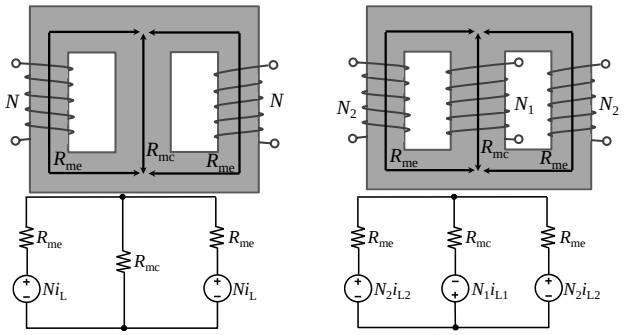
where I_{ph} and ΔI_{ph} are the average and ripple current through each winding, respectively.

2.3.3 LCI converter

The modeling of coupled inductors in interleaved boost converters is more complicated than the one of conventional topologies. As Figure 2.1 and Figure 2.2 depict, the loosely-coupled inductor is composed of one core of three legs and two windings, each one of N turns [14]-[15]. In this context, the sectional area of the external legs of the core as a function of the duty cycle can be calculated from the maximum flux density reported in [14]-[15] as follows:

$$A_e = \frac{1}{B_{\max}}\left[\frac{NI_{ph}}{(1+2\alpha)R_{mo}} + \frac{1}{2}\frac{V_{in}D}{Nf_{sw}}\right] \tag{2.9}$$

where R_{mo} is the magnetic reluctance of the external legs, and α is defined as the ratio of R_{mc}/R_{mo}, where R_{mc} is the reluctance of the central leg. Figure 2.4(a) shows the magnetic model of the LCI magnetic component.



(a) LCI (b) IWCI

Figure 2.4. Magnetic circuit models.

Considering the behavior of the magnetic flux in the central leg, and based on the maximum flux density derived in [14]-[15], (2.10) shows the calculation of the sectional area when the duty cycle is lower than 0.5. In the same way, (2.11) shows the calculation for the case of duty cycles higher than 0.5.

$$A_c = \frac{1}{B_{\max}}\left[\frac{2NI_{ph}}{(1+2\alpha)R_{mo}} + \frac{1}{2}\frac{V_{in}D}{Nf_{sw}}\frac{1-2D}{1-D}\right] \tag{2.10}$$

$$A_c = \frac{1}{B_{\max}}\left[\frac{2NI_{ph}}{(1+2\alpha)R_{mo}} + \frac{1}{2}\frac{V_{in}}{Nf_{sw}}(2D-1)\right] \tag{2.11}$$

2.3.4 IWCI converter

Finally, the integrated winding coupled inductor is composed of one magnetic core with three different windings installed in each leg. Figure 2.4(b) shows the magnetic model of the IWCI component. The numbers of turns are N_1 for the central winding and N_2 for the

external windings (see Figure 2.1 and Figure 2.2). Consequently, and based on the overall modeling of this magnetic component and the maximum magnetic flux density derivation presented in [17]-[19], (2.12) shows the sectional area of the external legs for the cases of duty cycles lower than 0.5, and (2.13) shows the sectional area calculation for the external legs when the duty cycle is higher than 0.5. In this converter, the operating states are different for duty cycles lower or higher that 0.5, and thereby the sectional area calculation is different for both cases.

$$A_e = \frac{1}{B_{\max}}\left[\frac{(1+2\beta)N_2 I_{ph}}{(1+2\alpha)R_{mo}} + \frac{1}{2}\frac{V_{in}D}{(1+2\beta)N_2 f_{sw}}\left(1+\frac{\beta}{1-D}\right)\right] \tag{2.12}$$

$$A_e = \frac{1}{B_{\max}}\left[\frac{(1+2\beta).N_2 I_{ph}}{(1+2\alpha)R_{mo}} + \frac{1}{2}\frac{V_{in}D}{(1+2\beta)N_2 f_{sw}}\left(1+\frac{\beta}{D}\right)\right] \tag{2.13}$$

where β is defined as the ratio of N_1/N_2 and, for this particular volume study, it is set as β=1. This β is chosen due to the convenience of having the same number of turns because the height of the central and external legs is the same in regular EE cores. Furthermore, (2.14) shows the calculation of the sectional area of the central leg when the duty cycle is lower than 0.5; and, (2.15) shows the case for a duty cycle higher than 0.5.

$$A_c = \frac{1}{B_{\max}}\left[\frac{2(1+2\beta)N_2 I_{ph}}{(1+2\alpha)R_{mo}} + \frac{1}{2}\frac{V_{in}D}{(1+2\beta)N_2 f_{sw}}\frac{1-2D}{1-D}\right] \tag{2.14}$$

$$A_c = \frac{1}{B_{\max}}\left[\frac{2(1+2\beta)N_2 I_{ph}}{(1+2\alpha)R_{mo}} + \frac{1}{2}\frac{V_{in}}{(1+2\beta)N_2 f_{sw}}(2D-1)\right] \tag{2.15}$$

2.3.5 Volume and losses comparison

A comparison among the selected topologies was performed taking into account the geometric models of cores and windings, their loss models, and the magnetic flux modeling of each topology. This was possible by solving (2.7)-(2.15) with the evaluation of different number of turns, and the calculation of each variable with the parameters defined in Table 2.1.

Figure 2.5 shows the comparison between the volume of each inductor (or pair of inductors in the case of the interleaved converter) and their power losses. This comparison was made considering a varying number of turns in each inductor, because the number of turns influences the core size and the inductor losses (both core and copper losses). Thus, each of the dots on each line corresponds to a value of the number of turns. In addition, the increment of the number of turns produces a reduction in the total inductor volume in each converter. This behavior is generated by the winding-core dependency, where the

lower the number of turns, the larger the core size in order to accomplish the filtering requirements.

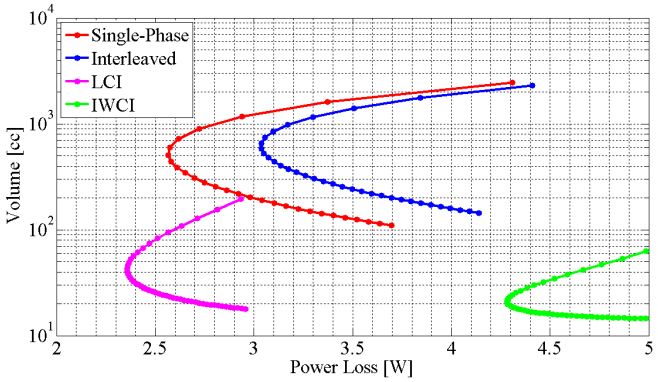


Figure 2.5. Inductor volume vs. inductor losses.

Figure 2.5 also shows that LCI and IWCI topologies offer low inductor volume. Moreover, the IWCI can be miniaturized compared with the LCI, but this miniaturization can lead to the increase in the inductor losses, this is because of the trade-off between the core size and the inductor losses. Additionally, it is possible to see the effectiveness of the magnetic coupling technique compared with the non-coupled inductors. Finally, the performance of the LCI converter is remarkable because it presents the lowest power losses with small volume for this case study. Therefore, the magnetic coupling technique is validated as an effective technique for downsizing and, in some cases, for increasing the efficiency of magnetic components.

2.4 Cooling Devices Volume

In order to calculate the volume of the cooling devices, the semiconductor losses and the heat sink modeling are required.

2.4.1 Semiconductor losses

Power losses in semiconductor devices can be classified into: switching and conduction losses that are dependent on the Equivalent Series Resistance (ESR), voltage drops, parasitic capacitances, and parasitic inductances, among others. [25]-[28].

In fact, transistor losses are produced by the static drain-source on-state resistance RDS(ON), the transistor input capacitance, the output capacitance, and the switching transition process. Diode losses are produced by the diode voltage drop, the diode resistance, and the reverse recovery when the converter operates in continuous conduction mode. The overall power loss model is explained in detail in [24].

Conventional Silicon and next-generation devices (Super Junction and SiC Devices) were chosen for evaluating their losses and thereby the volume of the required cooling devices. Table 2.2 shows the parameters of the selected semiconductors, taking into

account the voltage and current stresses of each topology. All the selected devices have a TO-247 package and a voltage rating of 650V for the Super-Junction devices and 600V for the other devices.

TABLE 2.2.Power Semiconductors Characteristics

Transistors	Mosfet	S-Jun	**Diodes**	Si Diode	SiC Diode
$R_{DS(ON)}$ [mΩ][1]	46.2	27.5	V_F [V] [1]	0.9	1.35
$R_{DS(ON)}$ [mΩ][2]	45.9	27	V_F [V] [2]	0.8	1.18
C_{iss}[pF] @200V	9600	9900			
C_{oss}[pF] @200V	350	190	Q_r [nC]	65	-
t_{rise} [ns]	52	27	t_{rr} [ns]	50	-
t_{fall} [ns]	81	5			

1 @ I_D=12.5 A, T_J=100°C [2] @ I_D=6.25 A, T_J=100°C

Based on the power loss model of [24], the parameters of Table 2.1 and the power semiconductors of Table 2.2, the individual power losses of the transistors and diodes of each converter are displayed in Table 2.3.

TABLE 2.3.Power Semiconductors Losses

Single-Phase		**Interleaved**		**LCI**		**IWCI**	
Transistor Losses [W]							
Si	S-Jun	Si	S-Jun	Si	S-Jun	Si	S-Jun
13.11	4.85	5.7	1.91	6.04	2.11	6.04	2.11
Diode Losses [W]							
Si	SiC	Si	SiC	Si	SiC	Si	SiC
13.28	7.75	5.78	3.2	5.78	3.2	5.78	3.2

2.4.2 Heat sink modeling

The first step to model the semiconductor cooling device (heat sinks are conventionally used for low power dissipation) is to calculate the required thermal resistance from the cooling device to the air [29]. This resistance can be calculated from the thermal circuit presented in Figure 2.6.

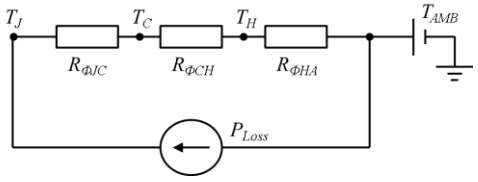


Figure 2.6. Thermal circuit.

The junction temperature T_J (defined by the manufacturer) can be calculated using (2.16).

$$T_J = T_{AMB} + (R_{\Phi JC} + R_{\Phi CH} + R_{\Phi HA})P_{Loss} \tag{2.16}$$

where T_{AMB} is the ambient temperature (usually 50°C for the ambient within the converter [30]), $R_{\Phi JC}$ is the thermal resistance from the junction to the semiconductor's case, $R_{\Phi CH}$ is the thermal resistance from the case to the heat sink (usually neglected due to its very small value), $R_{\Phi HA}$ is the thermal resistance from the heat sink to the air, and P_{Loss} is the dissipated power in each power device. Thus, using (2.16), it is possible to calculate the required heat sink thermal resistance.

All the selected power devices have a maximum junction temperature of 175°C; however, the heat sink volume calculation is conducted assuming a maximum junction temperature of 100°C with the purpose of protecting the power devices and preventing high ambient temperature rises.

Once the thermal resistance of the heat sink from the base plate surface to the ambient is calculated, the next step is to model the size of the heat sink. Figure 2.7 shows the definitions of the heat sink geometry, and based on [31]-[33], it is possible to derive the thermal resistance of the heat sink in relation to its geometry as follows:

$$R_{\Phi HA} = \frac{1}{n}\left[R_{th,d} + \frac{1}{2}\left(R_{th,FIN} + R_{th,A}\right)\right] + \frac{0.5}{\rho_{air} c_{P,air} V} \tag{2.17}$$

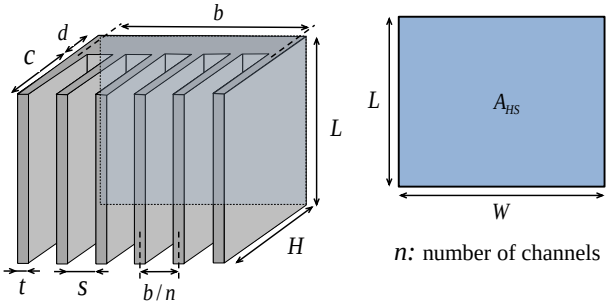


Figure 2.7. Heat sink geometry.

where n is the number of the channels, ρ_{air} is the air density, $c_{p,air}$ is the specific thermal capacitance of air, V is the air volume flow, and $R_{th,d}$ is the thermal resistance of the heat sink base of height d. $R_{th,d}$ is calculated as follows:

$$R_{th,d} = \frac{n.d}{A_{HS}\lambda_{HS}} \tag{2.18}$$

where A_{HS} is the size of the heat sink plate, and λ_{HS} is the thermal conductivity of the heat sink material (generally, heat sinks are manufactured with aluminum alloys). Additionally, $R_{th,FIN}$ is defined as the thermal resistance of the fins and is expressed as:

$$R_{th,FIN} = \frac{c}{tL\lambda_{HS}} \tag{2.19}$$

where c, t and L are the dimensions of the defined heat sink geometry. Finally, $R_{th,A}$ is the thermal resistance between the fin surface and the air channel:

$$R_{th,A} = \frac{1}{hLc} \tag{2.20}$$

where h is the convective heat transfer coefficient. The required heat sink dimensions, and thereby its volume, can be calculated by solving (2.17) according to (2.18)-(2.20). This calculation is made using the heat sink parameters shown in Table 2.4. Note that (2.17) presents several variables: s, L, t, d, c, and n. Based on several heat sinks, suitable for the TO-247 package and available in the market, the dimensions s, L, t, d, and c were selected as it is shown in Table 2.4. Using the calculated thermal resistance for the heat sinks, it is possible to derive the number of channels n that the heat sink needs, and therefore its volume is estimated.

TABLE 2.4. Heat Sink Parameters and Dimensions

Parameters	Value	Dimensions	Value
h [W/(m²°C)]	25	s [mm]	4
λ_{HS} [W/(m°C)]	237	L [mm]	25
V [m³/s]	0.006	t [mm]	1
ρ_{AIR} [kg/m³]	0.99	d [mm]	2
$c_{p,AIR}$ [J/(kg°C)]	1010	c [mm]	10

2.5 Volume Comparison

2.5.1 Power devices

When next-generation devices are used instead of conventional Silicon semiconductors, a reduction in power losses and heat sinks volume is produced. Table V shows the volume of the heat sinks set (pair or single) needed to dissipate the losses of each individual semiconductor. This heat sinks set corresponds to one device in the case of the single phase, and two devices in the case of the other three topologies. As a result, the use of next-generation power devices can reduce the power losses and thereby the heat sink volume up to 60% in comparison with the conventional Silicon semiconductors for the case of the defined 1kW prototype.

In addition, in order to have a better understanding of the calculated volume, Table 2.5 reports also the Cooling System Performance Index (CSPI), defined as the power density capability of the cooling system, described in detail in [31].

Table 2.5.Heat Sink Volume

Single-Phase		Interleaved		LCI		IWCI	
Transistor Heat Sink Volume [cc]							
Si	S-Jun	Si*	S-Jun*	Si*	S-Jun*	Si*	S-Jun*
7.18	2.79	6.46	2.54	6.81	2.75	6.81	2.75
CSPI [°C /(W.Liter)]							
18.74	17.59	17.86	15.09	17.9	15.44	17.9	15.44
Diode Heat Sink Volume [cc]							
Si	SiC	Si*	SiC*	Si*	SiC*	Si*	SiC*
6.36	3.7	5.52	3.27	5.52	3.27	5.52	3.27
CSPI [°C /(W.Liter)]							
18.66	18.03	17.56	16.13	17.56	16.13	17.56	16.13

*Heat Sink Values of Interleaved, LCI and IWCI correspond to a pair of devices

2.5.2 Total volume

Based on the inductor and the cooling modeling described above, the total volume of the selected topologies under the defined parameters was calculated. Two comparisons were made. The first one compares the volume of the total converter when each magnetic component of the four converters has windings with N=20 turns. This comparison is shown in Figure 2.8. The second comparison shows the converters when the inductors have their lowest power losses (Figure 2.9). These comparisons were calculated using the values of the Super-Junction Mosfet and the SiC Diode, as well as their corresponding heat sinks. For the comparison of Figure 2.8 and Figure 2.9, conventional electrolytic capacitors were used.

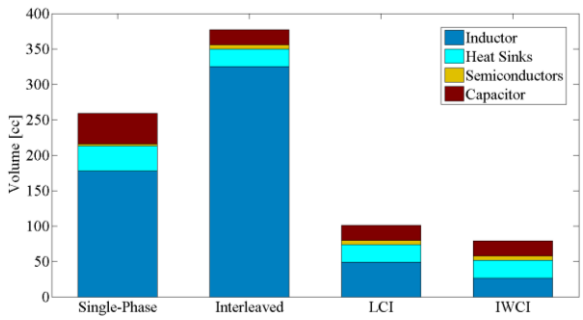


Figure 2.8. Total volume comparison when the inductors have 20 turns.

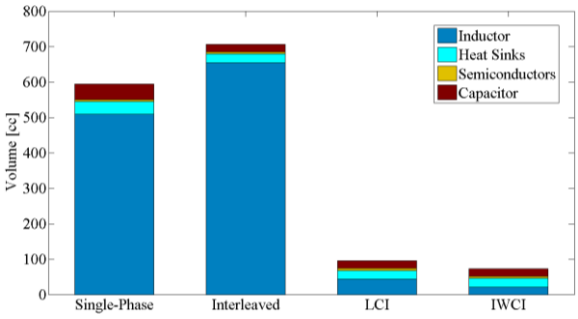


Figure 2.9. Total volume comparison at the lowest inductor losses.

Figure 2.5, Figure 2.8, and Figure 2.9 show the opposition between efficiency and power density, i.e., first, the topology that offers the lowest power losses is the LCI converter, and

second, this topology has a bigger volume in certain numbers of turns in comparison with the other three topologies. On the contrary, the IWCI converter exhibits the smallest volume, but for this case study, it presents the highest power losses.

2.6 Inductor Size Evaluation

In the previous sections, ideal cores with defined geometries (Figure 2.2) have been modeled. These geometries were defined using squares for calculation convenience. However, in practice, it is difficult to find the exact core that fills the design parameters. In this context, there are two possibilities: 1) To use a customized core that fulfills all the design requirements, resulting in an overcost due to the personalized core, or 2) To use a core available in the market that can fulfill the requirements. Consequently, in order to validate the modeling presented so far and compare the changes of efficiency and volume in the defined geometries with cores available in the market, four different cores were selected to be compared with the results exhibited in Figure 2.5. These cores were selected because their volume and effective sectional area fit into the calculated values of Figure 2.5, they are fabricated with the selected core material (TDK ferrite of reference PC40), and they offer a convenient trade-off between efficiency and volume based on Figure 2.5. In consequence, Figure 2.10 shows the core volume of the selected cores. These selected cores are represented in the comparative figure of inductor losses vs. core volume of each inductor (or pair of inductors in the case of the non-coupled interleaved converter).

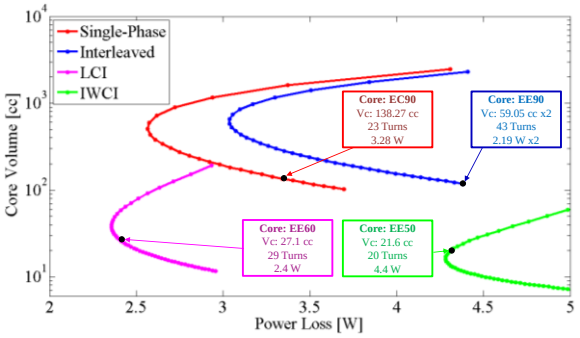
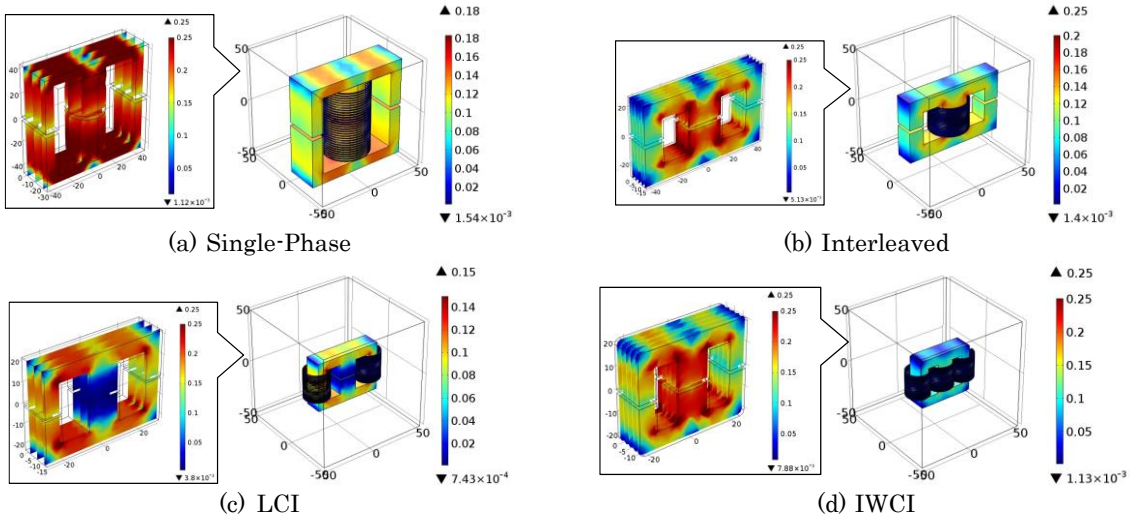


Figure 2.10. Core volume vs. inductor losses.

Figure 2.10 shows that non-coupled inductors (Single-Phase and Interleaved) require large cores to obtain the required filtering. Therefore, the region of considerable large number of turns (where the points represent a volume smaller than 200cc) is suitable for this study because huge core volumes are required for the region of few winding turns (a volume larger than 200cc). In addition, EC90 and EE90 cores are selected for the Single-Phase and the interleaved inductors, respectively. These cores were selected taking into account Figure 2.10 where their volume matches with the region of suitable core sizes. It is important to mention that the interleaved converter with non-coupled inductors (Blue line in Figure 2.10) uses two cores, obtaining a total core volume of 118.1cc for the case of two EE90 cores.

Additionally, magnetic coupled inductors can be made with smaller cores. EE60 core was selected for the case of the LCI, and EE50 for the IWCI.

In order to validate this modeling procedure, a Finite Element Method (FEM) was conducted for each inductor in order to check the magnetic flux density of each core and corroborate the saturation absence. Figure 2.11 shows the results of the FEM presenting the normal magnetic flux density in the surface of the cores. Figure 2.11 also shows the FEM results using slices of the cores in order to display the inner magnetic flux density. All the FEM results are presented in Teslas.



(a) Single-Phase (b) Interleaved

(c) LCI (d) IWCI

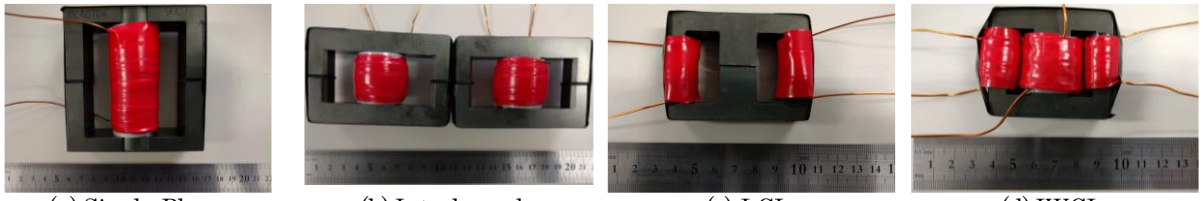
Figure 2.11. FEM results in Teslas.

Based on these results, the inductor modeling is validated because none of the models exceed 250mT (defined as the maximum magnetic flux density).

2.7 Experimental Results of the Volume Comparison

2.7.1 Inductors

In order to validate the volume comparison presented above, an experimental verification was conducted. This validation was carried out considering the results presented in Figure 2.10. As it was explained before, the volume comparison conducted in section V was made using custom core geometries; however, only specific cores could be used for the experimental validation due to access restriction of geometries available in the market. In this context, the experimental tests were performed using the cores evaluated in the previous section: EC90, EE90, EE60 and EE50 (Ferrites of reference PC40 manufactured by TDK). The setups of the prototypes of each inductor are shown in Figure 2.12. These prototypes were designed according to the method illustrated in sections II and III. Figure 2.12 clearly shows the size difference between the inductors.



(a) Single-Phase (b) Interleaved (c) LCI (d) IWCI

Figure 2.12. Inductor prototypes.

2.7.2 Power devices

The power devices used for the prototypes were the Super-Junction Mosfet and the SiC Diode presented and described in Table 2.2. This selection was made based on the higher efficiency performance of these components.

2.7.3 Heat sinks

As it is shown in section IV, the heat sink modeling was made with custom geometries. Although the heat sink parameters and dimensions of Table 2.4 were chosen based on real parameters of regular heat sinks for TO-247 packages, the total estimated volume is slightly different from the heat sinks available in the market. Therefore, the selected heat sinks are described as follows: Single-Phase's Mosfet: 7.9cc, 16.5°C/W; Single-Phase's Diode: 9.4cc, 14.2°C/W; All devices of the two-phase topologies (Interleaved, LCI and IWCI): 4.9cc, 22.2°C/W.

All the selected heat sinks present a thermal resistance slightly higher than the one calculated in section IV. This means that the junction temperature will be lower than the designed 100°C. In addition, the selected heat sinks present larger volume than the designed ones because only net volume (without dead space) was considered in the analytical design of section IV.

2.7.4 Capacitors

In order to select a suitable capacitor for the prototypes, MultiLayer Ceramic Capacitors (MLCC), Metallized Polypropylene Film, and Electrolytic capacitors were compared. The required capacitance is approximately 300µF and 150 µF for the single-phase and the two-phase converters, respectively. Therefore, capacitors with a capacitance nearby to 50µF were compared. Figure 2.13 shows the selected capacitors. Table 2.6 shows the specifications of the selected converters. It is possible to highlight in Table 2.6 the low ESR of the Film and the MLCC capacitors, the small volume of the MLCC and Electrolytic capacitors, and the large ESR of the electrolytic capacitor.

Table 2.6. Capacitor Comparison

Specification	Film	Electrolytic	MLCCx2
Capacitance [µF]	50	47	30*x2*
Rated Voltage [V]	500	400	400
ESR [mΩ] *Datasheet*	4	--	1 *each*
ESR [mΩ] *Measured*	5.65	416	2.8 *each*
Volume [cc]	56.7	4.02	2.37*x2*
PCB Area [cm²]	12.6	2.56 (*square*)	7.82*x2*

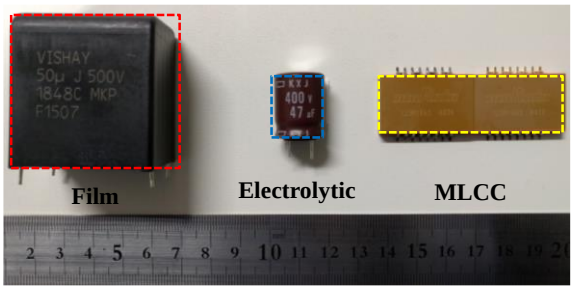


Figure 2.13. Capacitor comparison.

Although the volume of the electrolytic and the MLCC capacitors is really similar (4.02 vs. 4.74cc), the required PCB area of both capacitors is different (2.01 vs. 11.84cm^2). Therefore, electrolytic capacitors were chosen because they require much less PCB area leading to a more compact prototype in comparison to the case of the MLCC.

2.7.5 Volume evaluation

Figure 2.14 shows the prototypes of the four converters made with the selected components described before. The gate drivers were made using surface mount components with the purpose of reducing the volume. Figure 2.14 shows the volume difference between the prototypes. Each figure presents a Pie chart where the measured volume of each component group is presented. As Figure 2.8 and Figure 2.9 presented, it is confirmed that the inductor volume of the single-phase and the interleaved converters represents more than the 75% of the total prototype volume.

As a matter of fact, the largest volume of the four prototypes was presented by the single-phase topology (335.3cc). Note that in Figure 2.8 and Figure 2.9 the largest calculated volume was exhibited by the interleaved two-phase converter. Nevertheless, the analytical comparison presented in section V was made using net values without considering dead spaces between the heat sinks or inside the inductors. In practice, the prototype of the single-phase converter presents the largest volume because the window volume (dead space) of the EC90 is much bigger than the one of the two EE90 cores (82cc vs. 19cc, respectively). Conclusively, the interleaved two-phase topology is better in volume terms because it is more compact than the single-phase converter.

Finally, having the measured volume of each topology (Figure 2.14) and knowing that the prototypes were designed for 1kW, it is possible to calculate the power density of each prototype as follows: Single-Phase: 2.98W/cc; Interleaved: 3.36W/cc; 8.4W/cc; and IWCI: 9.66W/cc.

In conclusion, the volume comparison and the sizing modeling, presented in sections III, IV and V, are validated. It was confirmed that IWCI offers the highest power density due to the effect of the interleaving phases and the magnetic coupling techniques.

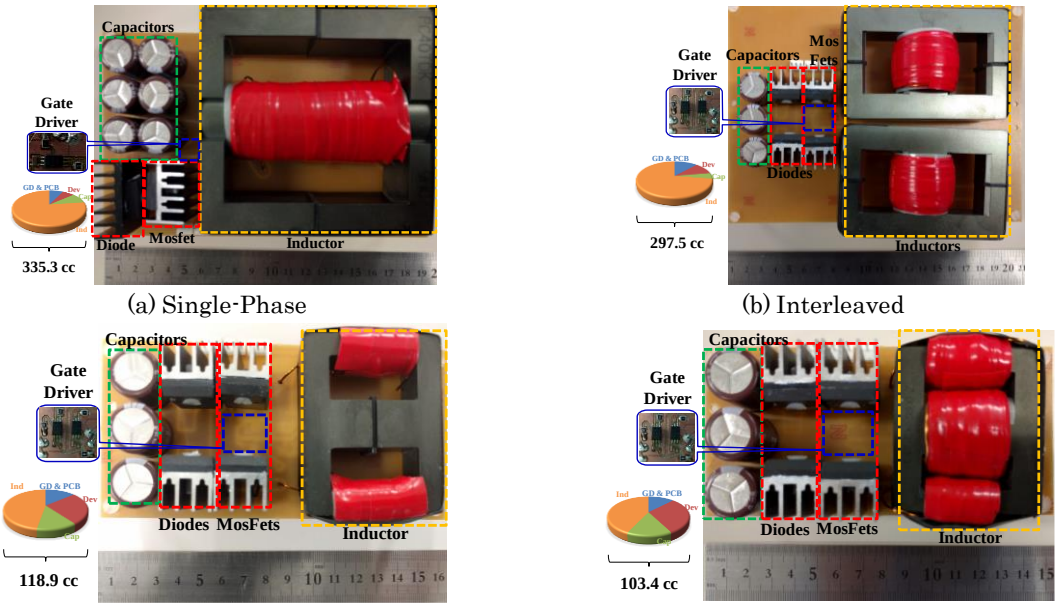


Figure 2.14. Prototypes of the four converters.

2.7.6 Experimental results

Figure 2.15 shows the experimental waveforms of the LCI converter tested with a 1kW load. From this figure, the current balancing is confirmed because the current peaks of both phases represented in the input current are almost the same. Also, it was confirmed that magnetic saturation in the magnetic components did not occur and a stable operation was realized. Therefore, the accuracy of the inductor design is validated from the experimental results.

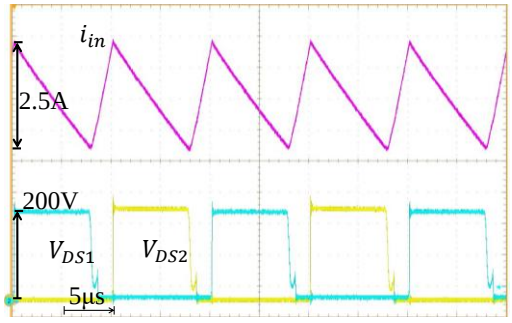


Figure 2.15. Experimental waveforms of the LCI prototype.

The efficiency of the LCI converter was measured with the conditions presented in Table 2.1, and a 98.05% of efficiency was measured at 1kW. Figure 2.16 shows the efficiency scanning from 200W until 1kW of the LCI converter.

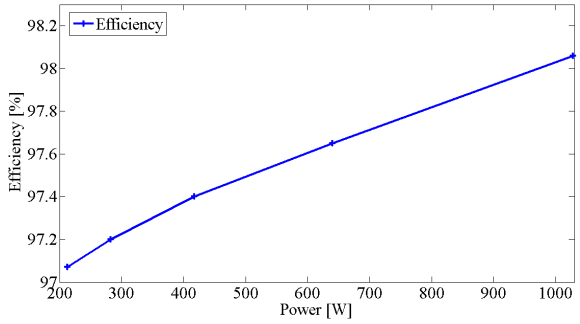


Figure 2.16. Efficiency measurement of the LCI converter.

In addition, Figure 2.17 shows the temperature rise of the heat sinks attached to the power devices of the LCI converter, where a maximum temperature of 73°C was measured after 11 minutes of testing.

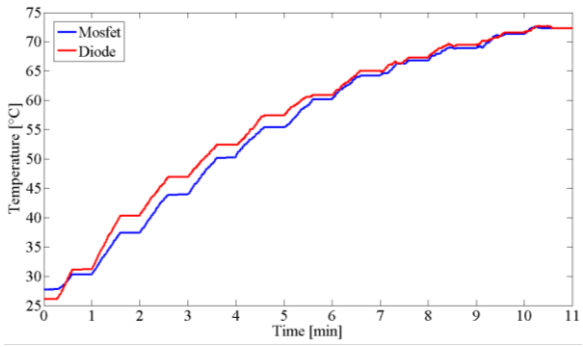


Figure 2.17. Temperature rise in the power devices of the LCI converter.

2.8 Short-Circuited Winding Technique

As it was explained above, the LCI converter shows an outstanding downsizing characteristic, specifically for magnetic components. Nevertheless, the design of this coupled-inductor is complicated. Usually it is designed by adjusting the coupling coefficient in order to realize the design parameters. However, the coupling coefficient is saturated by the fringing fluxes in the central leg and the external leakage fluxes.

These fluxes manly cause electromagnetic induced noises and the reduction of the downsizing performance. Consequently, to solve this problem, this section proposes the Short-Circuited Winding (SCW) technique.

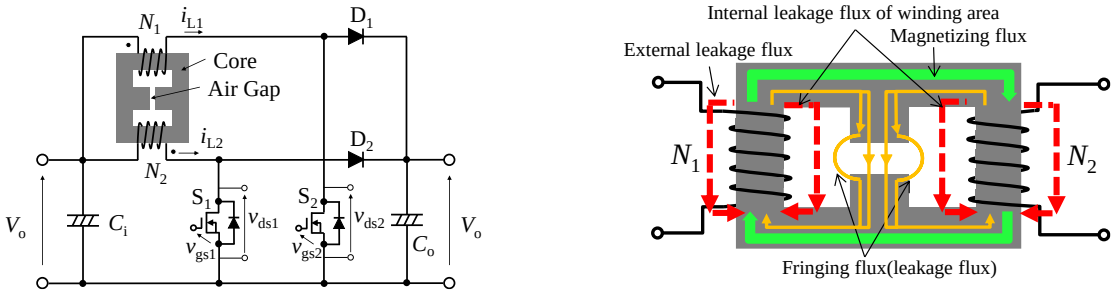
Generally speaking, coupled inductors that use magnetic cores such as EE or EI shapes presents the following three problems. 1) There are external leakage fluxes in the windings, and these fluxes affect the other components by the generation of Electromagnetic Induced (EMI) noise if the winding is installed near the other components. Even if there is a solution where the inductor can be arranged far from the

other components, the power-density packaging might be reduced. 2) Additional winding losses due to the fringing flux near the airgap can occur by a long airgap in the central leg. 3) If the coupling coefficient is saturated by these leakage fluxes, an airgap has to be inserted into the external legs. However, this solution produces a smaller mutual inductance, and a larger magnetizing current in the transformer. As a result, the efficiency may be decreased.

On the other hand, the reduction in the downsizing performance of the coupled inductor has to be considered. This is because the leakage inductance which is proportional to the DC fluxes has to be increased when the inductor current ripple of the circuit specifications is satisfied. To solve this problem, EIE core structure, designed to suppress fringing flux, has already been proposed in [25]. However, this core structure needs three parts of magnetic cores to configure the EIE structure. Therefore, the SCW technique is introduced. This SCW approach is effective for reducing the external leakage flux which is one of the causes of the EMI noise to other components [34].

2.8.1 Short-circuited winding approach

The interleaved boost converter with LCI is shown in Figure 2.18(a) and the magnetic core structure of the conventional LCI is shown in Figure 2.18(b). In the coupled inductor, there are external leakage fluxes of the windings and the fringing flux at the airgap as well as the magnetizing flux between each winding. The saturation of the coupling coefficient is caused by the fringing flux and the external leakage flux in the case of an EE core.



(a) Circuit configuration (b) Type of magnetic flux

Figure 2.18. LCI converter.

The aim of the SCW is to surround the magnetic core, see Figure 2.19. In this way, the internal fluxes, including the fringing flux and the magnetizing flux, do not affect the SCW because the total interlinkage fluxes do not change. However, only the external leakage fluxes have an effect inducing currents into the SCW. Therefore, the external leakage fluxes are canceled by the induced current into the SCW. Consequently, a high coupling coefficient by the short airgap length and the effect of the electromagnetic shield for the external leakage flux can be achieved.

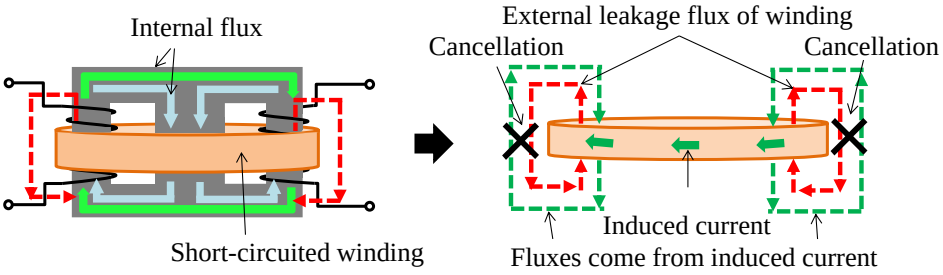


Figure 2.19. Coupled inductor surrounded by a short-circuited winding.

2.8.2 Experimental results of the SCW

To show the effectiveness of the SCW for the coupled inductor, an experimental evaluation was carried out. The evaluation circuit parameters and the magnetic parameters are shown in Table 2.7 and Table 2.8, respectively. The inductor ripple current and the flux density are designed at 1.5A and 250mT, similarly as the volume evaluation presented before. To obtain these parameters, a design method that satisfies both the inductor current ripple and the flux density is applied [34]. The design value and the measured value using the SCW and a conventional inductor are shown in Table 2.8.

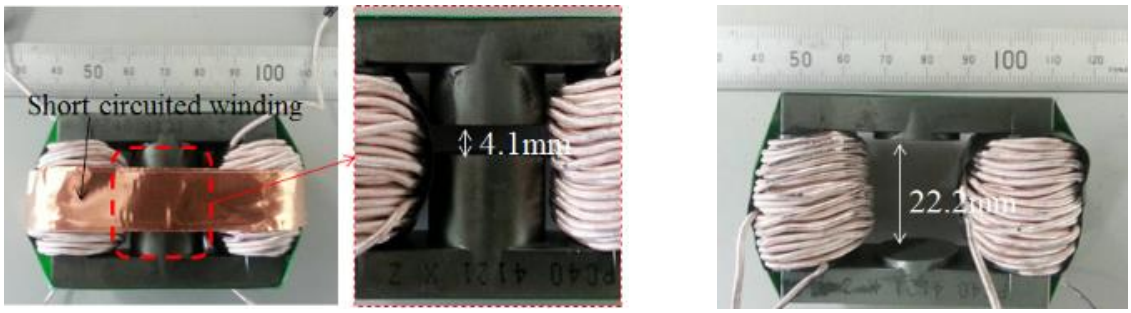
Table 2.7.Circuit Parameters of the Interleaved Boost Converter

Input voltage	V_i	140V
Output voltage	V_o	390V
Switching frequency	f_s	100kHz
Inductor ripple current	I_{Lpp}	1.5A
Output power	P_o	700W

Table 2.8. Magnetic Parameters

Magnetic core		PC40EER49(TDK)
Number of turns	N	44 turns
Maximum flux density	B_{max}	250mT
Designed value		
Mutual inductance	M	4.4mH
Leakage inductances	L_{lk1}, L_{lk2}	138μH
Measured values		
Proposed loosely coupled inductor with a short circuited winding		
Mutual inductance	M	4.5mH
Leakage inductances	L_{lk1}, L_{lk2}	139μH, 140μH
Air-gap length in the central leg		4.1mm
Conventional coupled inductor without a short circuited winding		
Mutual inductance	M	4.5mH
Leakage inductances	L_{lk1}, L_{lk2}	150μH, 148μH(Saturation)
Air-gap length in the central leg		22.2 mm

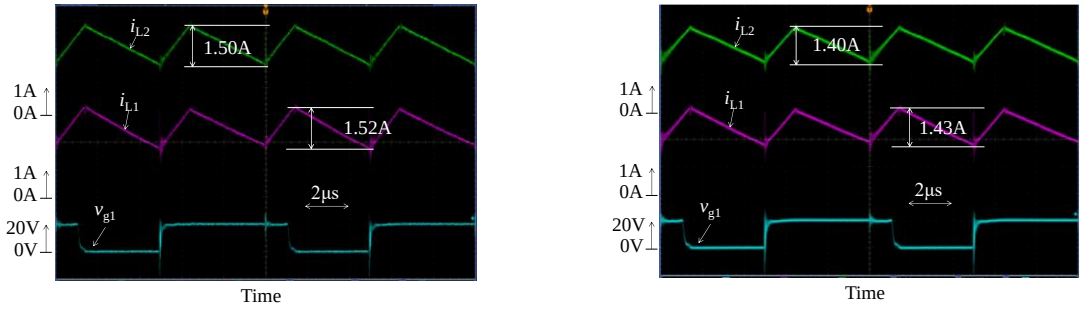
In addition, the prototype of coupled inductors is shown in Figure 2.20. The airgap length of the LCI with SCW can be reduced in comparison with the conventional LCI without SCW. Therefore, this SCW approach contributes to improve the coupling coefficient. Additionally, the leakage inductance of the conventional coupled inductor is saturated around 150μH. These values are different from the designed value of 140μH. Therefore, the conventional loosely coupled inductor cannot obtain any leakage inductance with high mutual inductance.



(a) With short-circuited winding (b) Without short-circuited winding

Figure 2.20. Prototypes of coupled inductors with short-circuited winding.

Figure 2.21(a) and Figure 2.21(b) show the experimental waveforms under the conditions of Table 2.7. From (a), (b), the proposed method fulfills the ripple current. Moreover, the conventional coupled inductor could not realize the design specification because of the external leakage flux.



(a) With short-circuited winding (b) Without short-circuited winding

Figure 2.21. Experimental waveforms.

Figure 2.22 shows the power conversion efficiency when the windings of the SCW use Litz wire to thin-film winding instead of the conventional wires. The reasons why Litz wire or thin-film winding are applied to the SCW is to reduce the AC resistance R_{AC} in the SCW and to improve the power conversion efficiency. From Figure 2.22, the power conversion efficiency is improved if the number of winding turns for the SCW is increased.

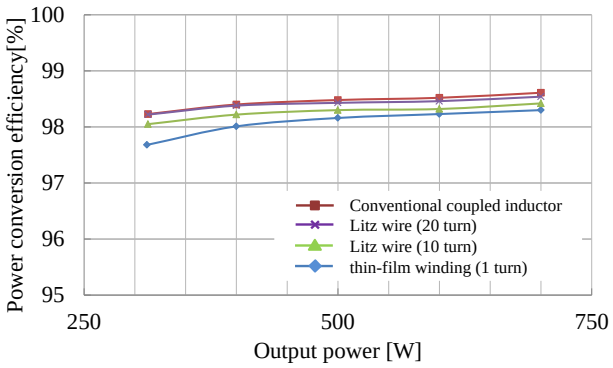
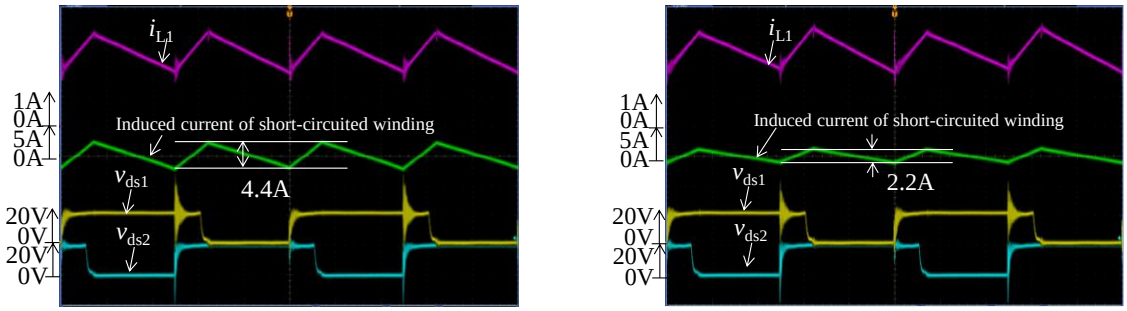


Figure 2.22. Converter efficiency using the short-circuited winding.

If the SCW approach is used, the power conversion efficiency can be decreased due to the winding losses of the SCW. However, if the number of turns is increased, the induced current can be reduced as shown in Figure 2.23. Therefore, the power conversion efficiency is improved in comparison with the case of few turns. If the AC resistance is close to the DC resistance of the SCW using Litz wire or thin-film winding, an increment in the turns of the SCW is effective for realizing the improving power conversion efficiency of the converter and keeping the electromagnetic shielding effect even if R_{AC} is increased by the winding length.



(a) Litz wire 10 turns (b) Litz wire 20 turns

Figure 2.23. Experimental waveforms including induced current.

2.9 Conclusions

A volume modeling methodology of four DC-DC converter topologies, combining geometry sizing, inductor modeling, power loss evaluation, and heat sinks modeling of conventional and next-generation devices, was proposed in this section. As a result, interleaving-phases and magnetic coupling techniques were validated as effective techniques to downsize the volume of DC-DC converters. For the 1kW case study presented in this article, the IWCI converter offered the smallest volume in comparison with other studied topologies. Additionally, this research suggests that the LCI converter is effective for reducing the size and improving the efficiency, and IWCI can further reduce the size but it can lead to increase in the magnetic losses. These facts make magnetic coupling and

interleaving phases as suitable techniques to be applied in the DC-DC converters of EVs, HEVs and FCEVs.

It was confirmed that the use of next-generation power devices can reduce the power losses and thereby the heat sink volume up to 60% in comparison with the conventional silicon devices. Moreover, based on the experimental results, a 98.05% of efficiency and a power density of 8.4 W/cc was measured in the LCI prototype.

The proposed methodology can be used for a designer of DC-DC converters, intended to be applied in electric mobility applications, because it gives an overall understanding of the effect of the characteristics of each component on the volume and efficiency of the entire converter. Moreover, the methodology can be used as a part of an optimization procedure of the converter, e.g. a multi-objective optimization of the volume, efficiency and temperature of the converter.

Finally, the Short Circuit Winding is introduced in order to increase the efficiency of magnetic integrated inductors by reducing the effect of the fringing flux. This approach was validated with experimental tests obtaining a 98.5% of efficiency.

References

[1] Y. Suh, T. Kang, H. Park, B. Kang and S. Kim, "Bi-directional Power Flow Rapid Charging System Using Coupled Inductor for Electric Vehicle," *IEEE Energy Conversion Congress and Expo (ECCE)*, pp. 3387-3394, 2012.

[2] K. Katsura and M. Yamamoto, "Optimal stability control method for transformer-linked three-phase boost chopper circuit," *IEEE Energy Conversion Congress and Exposition (ECCE),* pp. 1082–1087. 2012.

[3] M. Yilmaz and P. Krein, "Review of Battery Charger Topologies, Charging Power Levels, and Infrastructure for Plug-In Electric and Hybrid Vehicles," *IEEE Trans. on Power Electronics,* vol. 28, no. 5, pp. 2151-2169, May. 2013.

[4] Y. Cheng, R. Trigui, C. Espanet, A. Bouscayrol, and S. Cui, "Specifications and Design of a PM Electric Variable Transmission for Toyota Prius II," *IEEE Trans. on Vehicular Technology*, vol. 60, no.9, pp.4106-4114, Nov. 2011.

[5] W. Martinez, C. Cortes and L. Munoz, "Sizing of Ultracapacitors and Batteries for a High Performance Electric Vehicle," *IEEE International Electric Vehicle Conference (IEVC),* pp. 535-541. 2012.

[6] J. Gu, J. Lai, N. Kees, and C. Zheng, "Hybrid-Switching Full-Bridge DC–DC Converter with Minimal Voltage Stress of Bridge Rectifier, Reduced Circulating Losses, and Filter Requirement for Electric Vehicle Battery Chargers," *IEEE Trans. on Power Electronics*, vol. 28, no.3, pp.1132-1144, Mar. 2013.

[7] M. Pavlovsky, G. Guidi and A. Kawamura, "Assessment of Coupled and Independent Phase Designs of Interleaved Multiphase Buck/Boost DC–DC Converter for EV Power Train," *IEEE Trans. on Power Electronics*, vol. 29, no.6, pp. 2693-2704, Jun. 2014.

[8] F. Yang, X. Ruan, Y. Yang, Z. Ye, "Interleaved Critical Current Mode Boost PFC Converter with Coupled Inductor," *IEEE Trans. Power Electron.*, vol.26, no. 9, pp. 2404-2413, 2011.

[9] M. Hirakawa, Y. Watanabe, M. Nagano, K. Andoh, S. Nakatomi, S. Hashino and T. Shimizu, "High power DC/DC converter using extreme close-coupled inductors aimed for electric vehicles", *IEEE International Power Electronics Conference (IPEC)*, pp. 2941-2948, 2010.

[10] L. Tang and G. Su, "An Interleaved Reduced-Component-Count Multivoltage Bus DC/DC Converter for Fuel Cell Powered Electric Vehicle Applications", *IEEE Trans. on Industry Applications*, vol. 44, no. 5, pp. 1638-1644, Sep. 2008.

[11] W. Martinez and C. Cortes, "Design a DC-DC Converter for a High Performance Electric Vehicle," *IEEE International Conference on Connected Vehicles and Expo (ICCVE)*, pp. 335-340, 2012.

[12] W. Wen, Y. Lee, "A two-channel interleaved boost converter with reduced core loss and copper loss," *IEEE 35th Annual Power Electronics Specialists Conference (PESC)*, pp. 1003-1009, 2004.

[13] W. Martinez and C. Cortes, "High Power Density Interleaved DC-DC Converter for a High Performance Electric Vehicle," *IEEE Workshop on Power Electronics and Power Quality (PEPQA)*, pp. 1-6. 2013.

[14] M. Hirakawa, M. Nagano, Y. Watanabe, K. Andoh, S. Nakatomi and S. Hashino, "High Power Density DC/DC Converter using the Close-Coupled Inductors," *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.1760-1767, 2009.

[15] J. Imaoka, W. Martinez, S. Kimura, and M. Yamamoto, "A Novel Integrated Magnetic Core Structure Suitable for Transformer-linked Interleaved Boost Chopper Circuit," *IEEJ Journal of Industry Applications*, vol. 3, no. 5, pp. 395-404. Sep. 2014.

[16] M. Hirakawa, M. Nagano, Y. Watanabe, K. Andoh, S. Nakatomi and S. Hashino and T. Shimizu, "High Power Density interleaved DC/DC Converter using a 3-phase integrated Close-Coupled Inductor set aimed for electric vehicle," *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.2451-2457, 2010.

[17] J. Imaoka, M. Yamamoto, K. Umetani, S. Arimura and T. Hirano. "Characteristics analysis and performance evaluation for interleaved boost converter with integrated winding coupled inductor," *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.3711-3718, 2013.

[18] W. Martinez, S. Kimura, J. Imaoka, M. Yamamoto, K. Umetani, S. Arimura and T. Hirano. "High Power Density DC-DC Converter for Home Energy Management Systems," *International Conference on Intelligent Green Building and Smart Grid (IGBSG)*, pp.1-6, 2014.

[19] K. Umetani, J. Imaoka, M. Yamamoto, A. Seikoh and T. Hirano, "Evaluation of the Lagrangian method for deriving equivalent circuits of integrated magnetic components: A case study using the integrated winding coupled inductor," *IEEE Energy Conversion Congr. Expo. (ECCE)*, pp. 419-432, 2013.

[20] S. Kimura, S. Aoto, J. Imaoka, M. Yamamoto, "Allowable Power Analysis for High Power Density DC-DC Converters using Integrated Magnetic Components," *IEEE Energy Conversion Congr. Expo. (ECCE)*, pp. 419-432, 2014.

[21] J. Muhlethaler, J. Biela, J. Kolar and A. Ecklebe, "Core Losses under the DC Bias Condition Based on Steinmetz Parameters," *IEEE Trans. on Power Electronics*, vol. 27, no. 2, pp. 953-963, Feb. 2012.

[22] A. Van den Bossche and V. C. Valchev. "Modeling Ferrite Core Losses in Power Electronics," *International Review of Electrical Engineering*, pp. 16-23, 2006.

[23] C. P. Steinmetz, "On the law of hysteresis," *Proc. IEEE*, vol. 72, pp.196-221, 1984.

[24] W. Martinez, M. Yamamoto, P. Grbovic and C. Cortes, "Efficiency Optimization of a Single-Phase Boost DC-DC Converter for Electric Vehicle Applications," *IEEE 40th Annual Conference of the IEEE Industrial Electronics Society. (IECON)*, pp. 1-6, 2014.

[25] W. Aloisi and G. Palumbo, "Efficiency model of boost dc–dc PWM converters: Research Articles," *International Journal of Circuit Theory and Applications,* pp. 495-502, Sep. 2005.

[26] Z. Ivanovic, B. Blanusa, and M. Knezic, "Power Loss Model for Efficiency Improvement of Boost Converter," *XXIII International Symposium on Information, Communication and Automation Technologies (ICAT),* pp. 1-6. 2011.

[27] S. Kang, H. Nguyen, D. Maksimovic and I. Cohen, "Efficiency characterization and optimization in Flyback DC-DC converters," *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 527-534, 2010.

[28] W. Eberle, Z. Zhiliang, L. Yan-Fei and P. Sen, "A Practical Switching Loss Model for Buck Voltage Regulators," *IEEE Trans. on Power Electronics,* vol.24, no.3, pp.700-713, Mar. 2009.

[29] A. Jain, R. Jones, R. Chatterjee, S. Pozder, H. Zhihong, "A Thermal modeling and design of 3D integrated circuits," *11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM),* pp. 1139-1145. 2008.

[30] D. Gerlach, D. Gerty, R. Mahalingam, Y. Joshi, and A. Glezer, "A Modular Stackable Concept for Heat Removal from 3-D Stacked Chip Electronics by Interleaved Solid Spreaders and Synthetic Jets," *IEEE Trans. on Advanced Packaging,* vol 32, no. 32, pp. 431-439. 2009.

[31] U. Drofenik, G. Laimer, and J. W. Kolar, "Theoretical Converter Power Density Limits for Forced Convection Cooling," *International PCIM Europe Conference*, pp.608-619, 2005.

[32] U. Drofenik, and J. W. Kolar, "Analyzing the Theoretical Limits of Forced Air-Cooling by Employing Advanced Composite Materials with Thermal Conductivities > 400W/mK," *4th Conference on International Integrated Power Systems (CIPS)*, pp.1-6. 2006.

[33] U. Drofenik, A. Stupar and J. W. Kolar, "Analysis of Theoretical Limits of Forced-Air Cooling using Advanced Composite Materials with High Thermal Conductivities," *IEEE Trans. on Components, Packaging and Manufacturing Technology*, vol. 1, no. 4, pp.528-535. Apr. 2011.

[34] A. Yagasaki, "Highly Improved Performance of a Noise Isolation Transformer by a Thin-Film Short-Circuit Ring," IEEE Trans. on Electromagnetic compatibility, Vol. 41, No. 3, pp. 246-250, 1999.

3. Recovery-Less Boost Converter

3.1 Introduction

EVs applications have used conventional DC-DC topologies, like the well-known single-phase boost converter [1]-[2]. These conventional converters have some drawbacks that decrease the vehicle performance. Some of these drawbacks are: 1) switches and diodes are operated under hard switching which produce EMI/RFI noises and large switching losses [3]. 2) Large conduction losses in the windings and in the power devices are results of the large peak current generated when the voltage of the storage unit is quite lower than the output voltage. This behavior is presented due to the high duty cycle produced to obtain the required voltage-gain [4]-[5]. And, 3) Large mass and volume of the cooling system due to the additional components required for dissipating these losses described before [6].

An alternative to solve some of these problems is the use of the tapped-inductor DC-DC converter, shown in Figure 3.1. This converter offers the advantage of increasing the voltage-gain and reducing the voltage stress on the switch using one magnetic component where two windings are wounded [7]-[8]. Therefore, it is possible to achieve high power density and high voltage-gain using the magnetic coupling technique.

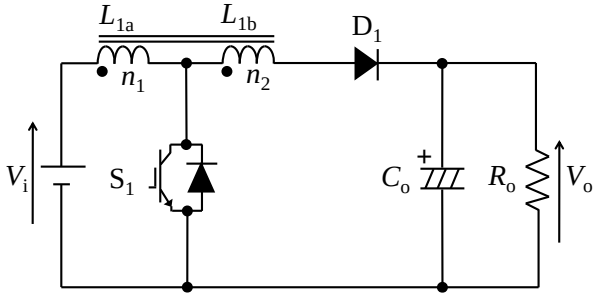


Figure 3.1. Tapped-inductor boost converter.

Integrated magnetic components have been often used in power converters to reduce the volume and the weight of their components [9]-[10]. Tapped inductors use this technique as they consist of two windings n_1 and n_2 magnetically coupled and wound into only one magnetic core. This characteristic offers the advantage of a high voltage-gain dependent on the ratio of the number of turns between the windings n_1 and n_2 [11]-[12]. The voltage-gain of tapped-inductor converters is expressed as follows:

$$M = \frac{V_o}{V_i} = \frac{1+ND}{1-D} \tag{3.1}$$

where V_o and V_i are the output and input voltage, respectively; D is the duty cycle of the gate signal in the power switch; and N is defined as the ratio of the number of turns in the primary and secondary windings in the tapped inductor:

$$N = \frac{n_2}{n_1} \tag{3.2}$$

The complete derivation process of Eq. (3.1) is described in [12]. However, despite the advantages highlighted, the conventional tapped-inductor topology presents some drawbacks: 1) Leakage inductances of the tapped-inductor, especially in winding n_2, produce high voltage spikes on the switch in the turning OFF process, which makes necessary high voltage rating devices with high ON resistance or high forward voltage; 2) EMI/RFI noises are generated by the steep performance of *di/dt* and *dv/dt*; 3) This topology operates at hard switching producing high switching losses.

In order to solve these problems, some improved tapped-inductor topologies with recovery-less performance are proposed in [13]-[17]. These converters use auxiliary inductors for reducing the reverse-recovery phenomenon. However, in some of them, the output voltage is not stable because the voltage-gain is dependent on the output load. In addition, the reverse-recovery reduction does not offer a considerable decrease of the switching losses in comparison to the conduction losses produced by the additional components. Thereby, the converter efficiency decreases in comparison to the hard-switching topology as is presented in [15].

In attention to this set of problems, in this section, a novel single-phase recovery-less boost converter with saturable inductors, capable of achieving high efficiency and volume reduction, is presented. This converter is inspired in the improved tapped-inductor converters proposed in [13]-[16]. The configuration and operating principle of this converter is introduced. Then, the suppression of the reverse-recovery phenomenon and the design procedure are introduced. In addition, the two-phase recovery-less boost converter is introduced as a solution to increase the efficiency of the conventional tapped-inductor converter. This way, the same tests are employed to analyze both the two-phase and the single phase recovery-less converter Finally, experimental test results of a 1kW prototype are shown as a validation of the presented topologies.

3.2 Conventional Tapped-Inductor Converter with Auxiliary Inductor

Figure 3.2 shows the conventional recovery-less boost converter with auxiliary inductor proposed in [13] and studied in [14]-[16]. This converter has a tapped-inductor divided into

the primary winding L_{1a} the secondary winding L_{1b} that are made with n_1 and n_2 turns, respectively, a main diode D_1, a bypass diode D_2, a switching transistor S_1, a smoothing capacitor C_o, and an additional inductor L_a connected between the secondary winding L_{1b} and the main diode D_1. This auxiliary inductor produces a small reduction of the reverse-recovery phenomenon and the suppression of the turning on losses in the switch because Zero Current Switching (ZCS) is achieved [14].

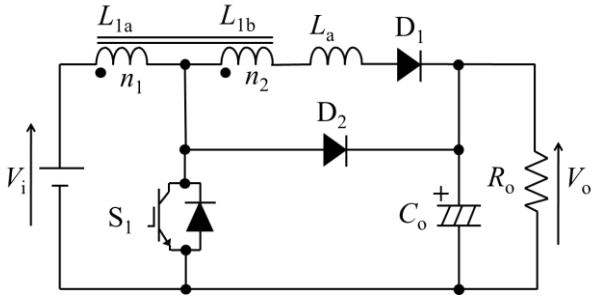


Figure 3.2. Conventional tapped-inductor converter with auxiliary inductor.

Moreover, in comparison with the conventional single-phase boost converter [17], this topology has only two additional components: the bypass diode D_2 and the auxiliary inductor L_a. No additional cores are required as the tapped inductor L_1 uses the same core of the conventional inductor required for the single-phase boost converter.

It is important to note the existence of variations of this topology that preserve a similar operation principle based on the operation of the auxiliary inductor. Such variations are related to the auxiliary inductor position. Some examples are explained in detail in [18]-[19].

This topology presents four operating modes based on the switching performance of S_1 and the operation of the auxiliary inductor. This way, [15] widely explains the operation of each mode, highlighting the operation of the auxiliary inductor and the bypass diode that produce a soft-switching performance in the main loop current when the switch is turned OFF. Additionally, when the switch is turned OFF, a soft commutation process takes place resulting from the stored energy of the auxiliary inductor that starts to decrease as the current through the switch increases. Therefore, the slope of the main diode current is not as high as the conventional boost converter, which helps to reduce the reverse-recovery phenomenon [13]-[16].

The recovery-less converter with auxiliary inductor presents some drawbacks that reduce the effectiveness of the converter to be used in EV applications. These problems are described as follows:

1. When the current flows from the bypass diode D_2 to the main diode D_1, the commutation time is longer at high power or high current condition than at lower current condition. Therefore, if the commutation does not finish during the OFF state, the recovery phenomenon will occur in the bypass diode D_2, due to the stored charge of the bypass diode. Nevertheless, this problem can be solved by two means. 1) Reducing the inductance of the

auxiliary inductor. However, the change rate of the current *di/dt* is increased and therefore the reduction effect of the recovery phenomenon is reduced; 2) Increasing the OFF time of the switch by increasing the winding turns n_2. However, this method increases the volume and the power losses of the tapped inductor.

2. Although this converter offers a reduction of the reverse-recovery phenomenon, this reduction is not significant enough to compensate the use of additional components. Therefore, as [15] shows, the efficiency of this topology is lower than the conventional boost converter operating at hard-switching condition.

Once described the problems mentioned above, a novel topology of recovery-less boost converter capable to realize a further reduction of the reverse recovery phenomenon is introduced.

3.3 Single-Phase Recovery-Less Boost Converter

In this section, the proposed recovery-less boost converter, that integrates the use of saturable inductors as a solution to the drawbacks described above, is presented and analyzed. It is important to mention that the use of saturable inductors to reduce the reverse-recovery phenomenon was introduced by [20] in a similar topology than the conventional recovery-less converter with auxiliary inductor. Nevertheless, the proposed converter offers a faster transition, due to the fact of using two saturable inductors, which produces a larger reduction of the reverse-recovery phenomenon. In addition, the proposed converter has fewer components which means a power density increasing.

As shown in Figure 3.3, the proposed recovery-less boost converter is a single-phase boost converter composed of a tapped inductor made of two windings L_{1a} and L_{1b}, a main diode D_1, a bypass diode D_2, a switching transistor S_1, a smoothing capacitor C_o and two particular auxiliary inductors L_{sat1} and L_{sat2}. These inductors are made with saturable characteristics. L_{sat1} is installed between L_{1b} and the main diode and L_{sat2} between the tap of the tapped-inductor and the switch. In comparison to the conventional recovery-less boost converter with auxiliary inductor, the proposed converter has an additional inductor.

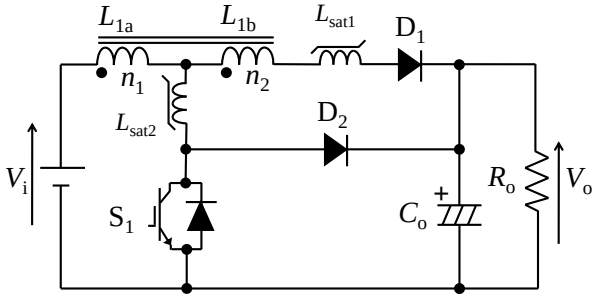


Figure 3.3. Single-phase recovery-less boost converter.

The novel recovery-less converter with saturable inductor has six operating modes corresponding to all the combinations of the ON and OFF states of the switch and the

transition modes generated by the saturable inductors and the bypass diode D_2. Figure 3.4 shows the voltage and current waveforms of each mode, and Figure 3.5 shows each operating mode.

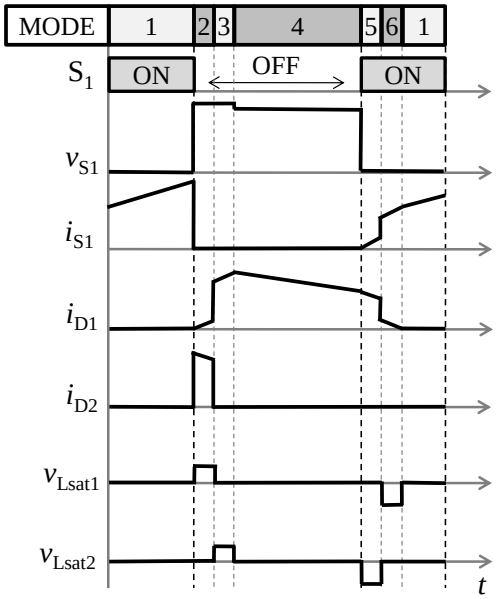


Figure 3.4. Voltage and current waveforms during each mode.

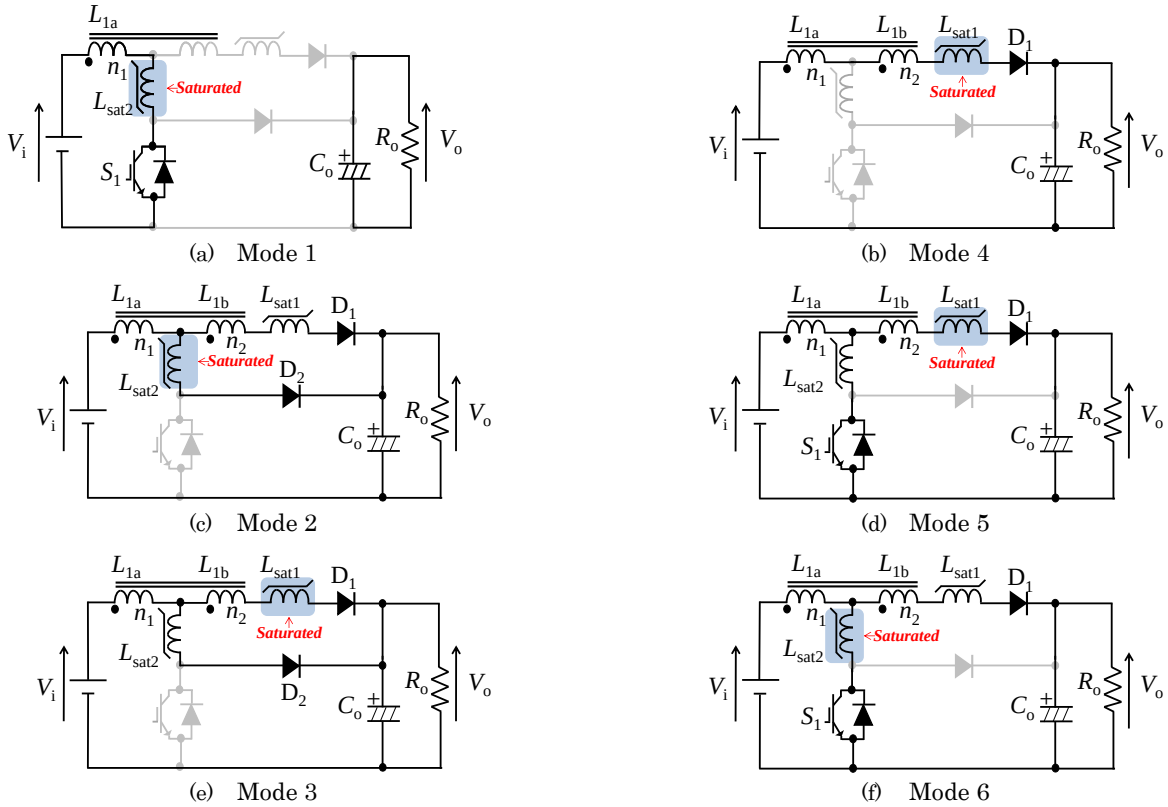


Figure 3.5. Operating modes.

Mode 1: As Figure 3.5(a) shows, S_1 is turned ON and the input current flows through the first winding of the tapped inductor L_{1a}, the auxiliary inductor L_{sat2} and the switch. The saturable inductor becomes saturated and the energy stored in the output capacitor is discharged onto the load.

Mode 2: Based on Figure 3.5(b), mode 2 corresponds to the short transition period immediately after S_1 is turned OFF. The input current is divided between the loop of the bypass diode D_2 and L_{sat2}, which continues in magnetic saturation, and the main loop of L_{sat1} and D_1. Due to the stored energy of L_{sat2}, the current through the bypass loop starts to decrease as the current through the main loop is increased.

Consequently, the slope of the current in the main loop is determined by the inductance of L_{1b} and L_{sat1}, which is not saturated yet. Therefore, the current flowing through the main diode D_1 is linearly increased from zero. Additionally, the output capacitor and the load are fed directly from the power supply across the main loop and the bypass loop. Finally, when the current flowing through the auxiliary inductor L_{sat2} reaches the point where the inductor leaves the saturation state, the change to Mode 3 occurs, as is shown in the voltage and current waveforms of Figure 3.4.

Mode 3: As Figure 3.5(c) shows, when the auxiliary L_{sat2} is not anymore saturated, a transition occurs where the majority of the input current starts to flow through the main loop and thereby the auxiliary inductor L_{sat1} becomes saturated.

At the same time the current through the bypass diode D_2 and the auxiliary inductor L_{sat2} decreases as the current of the main loop is increased.

This mode finishes when the energy stored in the auxiliary inductor L_{sat2} is totally discharged onto the output capacitor and the load. Therefore, it is possible to infer that the transition process between the ON and the OFF state of the switch finishes. In addition, the soft behavior of the main diode current i_{D1} is achieved, as Figure 3.4 shows.

Mode 4: As is shown in Figure 3.5(d), mode 4 presents a similar operation than the conventional tapped converter, where the input current totally flows through the tapped inductor and the main diode D_1, and it supplies the energy to the output capacitor and the load. In addition, the saturable inductor of the main loop L_{sat1} remains in saturation.

Mode 5: Based on Figure 3.5(e), mode 5 corresponds to the short transition period immediately after S_1 is turned ON, which is similar to the behavior of mode 2.

When S_1 is turned ON, the input current starts to flow through L_{sat2} and through the switch. Therefore, ZCS operation is achieved because the input current gradually increases through S_1 while the switch is already ON. Therefore, no turning ON losses are produced.

On the other hand, L_{sat1} is still under magnetic saturation and the current through the main diode D_1 starts to decrease as the current through the switch increases. Additionally, the output capacitor and the load are feeding directly only by the power supply across the main loop.

Finally, when this current flowing through the auxiliary inductor L_{sat1} reaches the point where the inductor leaves the saturation state, the change to Mode 6 occurs, as is shown in the voltage and current waveforms of Figure 3.4.

Mode 6: As Figure 3.5(f) shows, when the auxiliary L_{sat1} is out of saturation, a transition occurs where the majority of the input current starts to flow through the switch and thereby the auxiliary inductor L_{sat2} becomes saturated. In addition, the current through the main diode D_1 and the auxiliary inductor L_{sat1} decreases as the current of the switch is increased.

This mode finishes when the energy stored in the auxiliary inductor L_{sat1} is totally discharged onto the output capacitor and the load. Therefore, it is possible to infer that the transition process between the OFF and the ON state of the switch is finished.

3.3.1 Suppression of the recovery phenomenon

In order to show the advantage of the proposed converter in the recovery phenomenon suppression, the comparison to the conventional recovery-less boost converter with auxiliary inductor is carried out.

Consequently, Figure 3.6 shows the commutation current in the main diode D_1 and in the bypass diode D_2 of the conventional topology. This commutation period corresponds to the short transition period immediately after S_1 is turned OFF. As it is mentioned above, this topology produces a reduction of the recovery phenomenon which is dependent on the slope of the decreasing diode current. However, it is important to mention that this phenomenon is quite soft and produce lower recovery losses in comparison to the basic tapped boost converter [8].

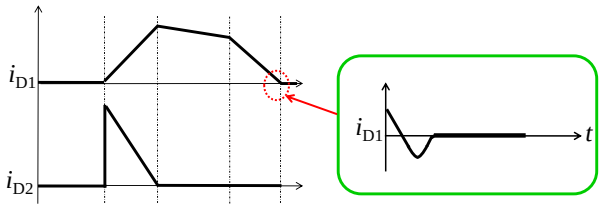


Figure 3.6. Commutation current in the conventional recovery-less boost converter with auxiliary inductor.

In contrast, the proposed recovery-less boost converter with saturable inductors shows a different transition behavior due to the presence of the auxiliary inductors and their saturable characteristic.

As shown in Figure 3.7, the commutation period between the ON and the OFF state of the switch presents one additional mode because of the presence of one additional auxiliary inductor and its saturable characteristic.

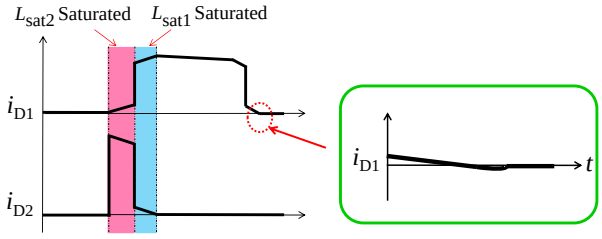


Figure 3.7. Commutation current in the proposed converter.

Therefore, as it was described above, Mode 2 occurs immediately after S_1 is turned OFF, the current through the bypass diode D_2 starts to decrease as the current through the main loop is increased. This mode is similar to the one of the conventional recovery-less boost converter with auxiliary inductor.

Nevertheless, the main difference between these two topologies is the presence of the second auxiliary inductor and it is evident in Mode 3, as is shown in the blue bar in Figure 3.7. In this mode, a transition occurs in the bypass diode D_2 and the current instantaneously decreases due to the presence of the saturable inductor in the main loop.

In fact, the slope of the change rating of the main and bypass current is determined by the value of the saturable inductors that is calculated considering the falling rate current of the selected diode di_D/dt.

Conclusively, the proposed method produces a rapid transition which is faster than the conventional recovery-less converter with auxiliary inductor, see the comparison between Figure 3.6 and Figure 3.7. Therefore, the recovery phenomenon is minimized because the reverse recovery time is very small due to the transition process generated by the saturable inductors. This characteristic offers the advantage of a highly reduction of the recovery loss in the main diode.

3.3.2 Design of the saturable inductors

As it was shown in section 3.3, where the suppression of the recovery phenomenon was presented, the objective of the saturable inductors is to reduce the transition time of the switch commutation and to soft the slope of the diode current. Therefore, the first step to design the saturable inductors is to define the value of reverse-recovery current that is desired to obtain in the main diode. Consequently, the characterization of the selected diode is required in order to obtain the relationship between the falling current rate and the recovery current produced. Figure 3.8 shows the characteristic curve of the selected diode. This curve can be obtained from the diode datasheet or by the conduction of a characterization procedure.

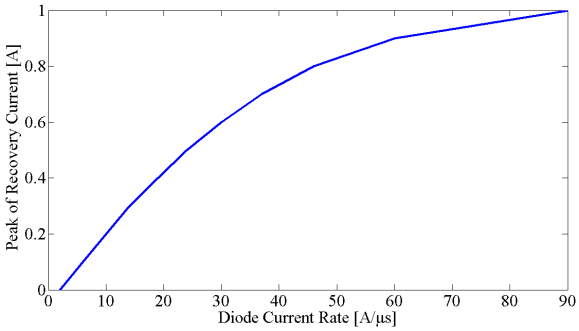


Figure 3.8. Diode current rate vs. peak of the recovery current.

Once the target of recovery current is defined, it is possible to find the required inductance by applying the following expressions.

$$L_{sat1} = \frac{n_1 V_o + n_2 V_i}{(n_1 + n_2)\, di_D/dt} \tag{3.3}$$

$$L_{sat2} = \frac{n_1 (n_1 V_o + n_2 V_i)}{(n_1 + n_2)^2\, di_D/dt} \tag{3.4}$$

These equations can be derived on the basis of the steady-state analysis of the proposed converter. Consequently, considering the operating modes shown in Figure 3.5 and described in section 3.2 it is possible to establish the voltages of each saturable inductor as follows:

$$v_{Lsat1} = V_o + \frac{n_2}{n_1} V_i \tag{3.5}$$

$$v_{Lsat2} = V_o - \frac{n_2}{n_1 + n_2} \left(V_i - V_o \right) \tag{3.6}$$

Simplifying (3.5) and (3.6), it is possible to obtain:

$$v_{Lsat1} = \frac{n_1 V_o + n_2 V_i}{n_1} \tag{3.7}$$

$$v_{Lsat2} = \frac{n_1 V_o + n_2 V_i}{n_1 + n_2} \tag{3.8}$$

Moreover, the reverse-recovery phenomenon during the turning-OFF process of the main diode can be suppressed taking into account the appropriate current falling rate di_D/dt. Therefore, the required inductance to ensure the current falling rate is derived as follows:

$$L_{sat1} = \frac{v_{Lsat1}}{di_D/dt} \tag{3.9}$$

$$L_{sat2} = \frac{n_1}{n_1 + n_2} \frac{v_{Lsat2}}{di_D/dt} \tag{3.10}$$

Therefore, replacing (3.7) in (3.9) and (3.8) in (3.10), it is possible to obtain:

$$L_{sat1} = \frac{n_1 V_o + n_2 V_i}{(n_1 + n_2)\, di_D/dt} \tag{3.11}$$

$$L_{sat2} = \frac{n_1 (n_1 V_o + n_2 V_i)}{(n_1 + n_2)^2\, di_D/dt} \tag{3.12}$$

Moreover, in order to select the suitable core and wire, a conventional method for inductors designing can be applied. However, for this specific case, the magnetic core must be designed to be saturated, therefore, the core size can be greatly reduced [21]

On the other hand, in order to compare the design procedure of the proposed converter with the conventional topology, [15] and [19] show the design procedure of the auxiliary inductor for the conventional topology. Consequently, the minimum value of the required inductance of the auxiliary inductor can be calculated by using the following expression:

$$L_{a-\min} = \frac{n_1 V_o + n_2 V_i}{n_1\, di_D/dt} \tag{3.13}$$

3.3.3 Experimental validation

In order to validate and to have a complete understanding of the effectiveness of the proposed recovery-less converter with saturable inductors, a 1kW prototype was constructed and experimentally tested. Additionally, a 1kW prototype of the conventional recovery-less converter with auxiliary inductor, explained in section 2, was constructed with the purpose of comparing the recovery phenomenon and the power density. Table 3.1 shows the parameters of each prototype and Figure 3.9 shows the experimental setup of the proposed converter.

Table 3.1. Design Parameters of the Conventional and the Recovery-Less Circuit

Parameter		Conventional	Recovery-Less
Input voltage [V]	V_i	100	100
Output voltage [V]	V_o	200	200
Tapped inductance [μH]	L_1	659	659
Auxiliary inductance [μH]	L_a	23.2	--
Saturable inductance [μH]	L_{sat1}	--	54.95
Saturable inductance [μH]	L_{sat2}	--	47.1
Switching frequency [kHz]	f_s	50	50
Output capacitance [μF]	C_o	60	60
Turns ratio	n_1:n_2	5:1	5:1

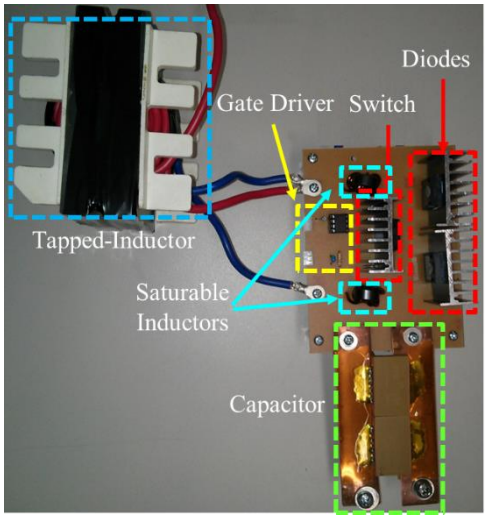


Figure 3.9. Experimental setup of the single phase recovery-less converter.

These prototypes were constructed with 600V Mosfets, 600V Silicon Diodes, Ferrite cores and Multilayered Ceramic Capacitors. As a result, Figure 3.10 shows the switch voltage and the input current of the proposed converter.

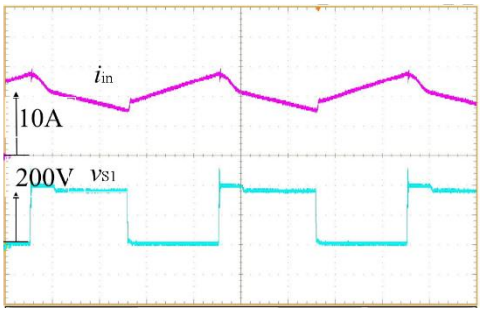


Figure 3.10. Switch voltage vs. Input current in the proposed converter.

- ***Size Comparison***

Figure 3.11 shows the size comparison of the auxiliary inductor used in the prototype of the conventional recovery-less converter and the two saturable inductors used in the proposed converter.

As a result, the auxiliary inductors used in the conventional converter have a cross sectional area of 0.48 cm^2, while the saturable inductors of the proposed circuit have a cross sectional area of 0.23 cm^2. Therefore, a total volume of the auxiliary inductor is 3.89 *cc* compared to the 1.42 *cc* of the two saturable inductors. As a conclusion, the proposed converter offers a reduction of 63.5% in the size of the auxiliary inductors even when the proposed converter used one additional inductor compared to the conventional circuit.

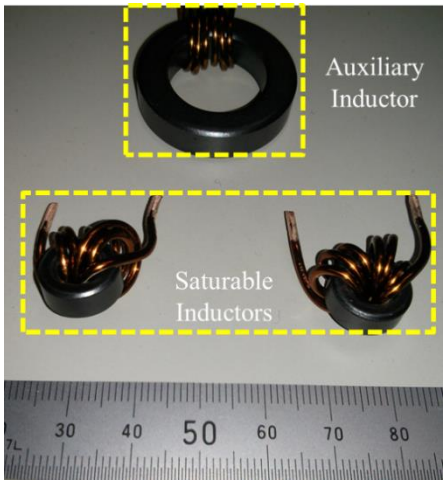
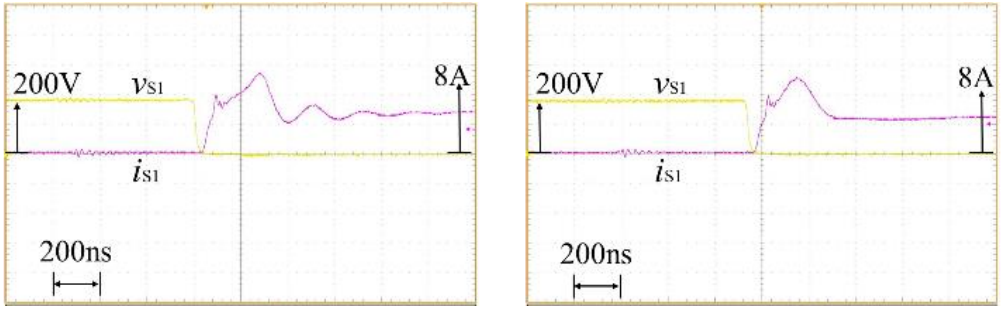


Figure 3.11. Inductor size comparison.

- ***ZCS Behavior***

Figure 3.12 shows the current and voltage waveforms of the switch when it is turned ON. Consequently, both topologies present ZCS behavior because in both circuits the drain-source voltage becomes zero while the current does not start to increase. Nevertheless, it is evident the noise reduction in the current waveform of the proposed converter due to the presence of the saturable inductors. In addition, the transition exhibited in the proposed converter is shorter.

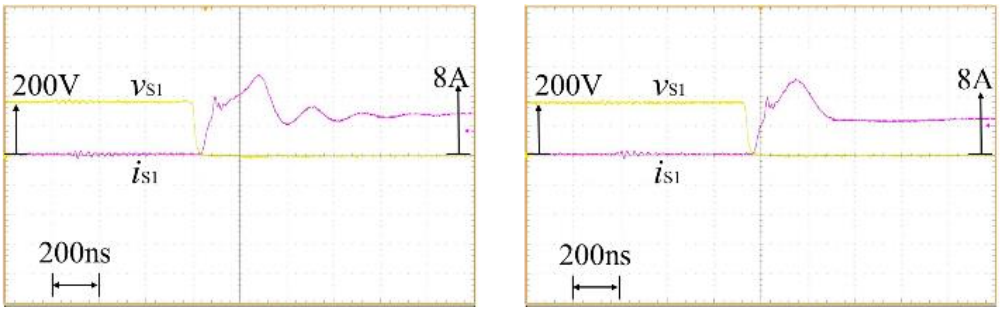


(a) Conventional circuit (b) Proposed circuit

Figure 3.12. Turning ON process of the switch.

- ***Reverse-Recovery Reduction***

Figure 3.13 shows the comparison of the current and voltage of the main diode. Therefore, it is possible to conclude that the proposed converter offers a reduction of the surge voltage in the main diode because the presence of the saturable inductor in the main loop produces a damped effect in the diode voltage due to the resonance of the inductance $Lsat_2$ and the internal capacitance of the diode.



(a) Conventional circuit (b) Proposed circuit

Figure 3.13. Reduction of recovery phenomenon in the main diode.

Therefore, the propose converter has a reverse-recovery current of 0.6A while the conventional circuit presents 2.2A. It means, a reduction of 72% in the reverse-recovery current.

- ***Efficiency***

Finally, with the purpose of having a better understanding of the advantages of the proposed converter, efficiency tests were made. Figure 3.15 shows the comparison of the total efficiency of the conventional and proposed recovery-less converters. Consequently, the proposed converter offers an outstanding performance in comparison to the conventional recovery-less topology. Specifically, the proposed converter offers an efficiency increment of approximately 1.2%. Where its maximum efficiency point is presented at 400W with a value of 97.55%.

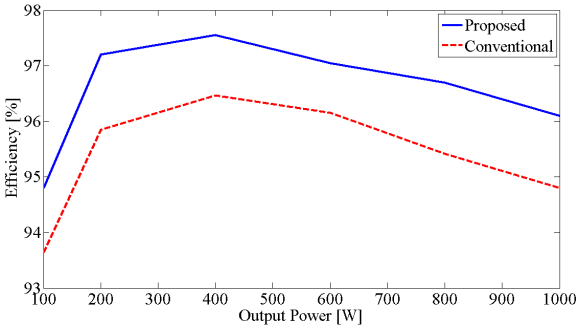


Figure 3.14. Efficiency comparison.

Moreover, comparing these results with the one presented in [15], it is possible to validate the effectiveness of the proposed converter that offers a higher efficiency in comparison to the conventional converter and the hard-switching converters.

3.4 Two-Phase Interleaved Boost Converter with Saturable Inductors

The two-phase tapped-inductor DC-DC converter was proposed as a solution for increasing the voltage-gain and reducing the voltage stress on the switch. This topology uses one magnetic component which reduces the volume and the complexity of the converter [22]. Therefore, it is possible to achieve high power density, high efficiency and high voltage-gain using the well-known magnetic coupling technique. Figure 3.1 shows the conventional tapped-inductor boost converter.

The tapped inductors of this converter have two windings n_1 and n_2 magnetically coupled due to the fact of these windings are wound in only one magnetic core. This characteristic offers the advantage of a high voltage-gain dependent on the ratio of the number of turns between the windings [23].

However, the conventional tapped-inductor topology presents some drawbacks: 1) Leakage inductances of the tapped-inductor, especially on winding n_2, produce high voltage spikes on the switch when it is turned OFF. Additionally, high losses are induced. 2) EMI/RFI noise is generated by the large slope of voltage and current waveforms. And, 3) This topology operates under hard switching operation that produces high switching losses [24]. As a consequence, the Zero Current Switching (ZCS) converter, proposed in [25]-[26] and shown in Figure 3.15, offers attractive features of increasing the efficiency, ZCS behavior and EMI/RFI reduction.

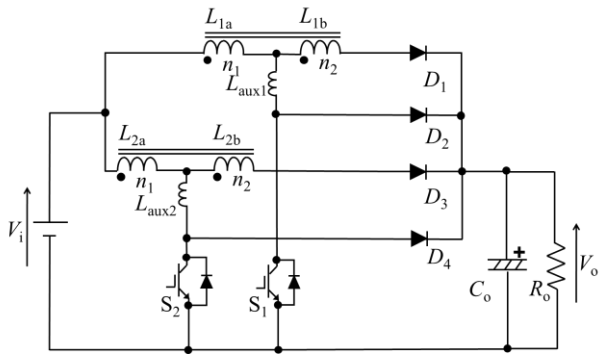


Figure 3.15. Conventional interleaved ZCS converter.

This converter is a two-phase interleaved boost converter composed of a tapped inductor made of two windings L_{1a} and L_{1b}, two main diodes $D_{1,3}$ two bypass diodes $D_{2,4}$, two switching transistors $S_{1,2}$, a smoothing capacitor C_o and two particular auxiliary inductors L_{aux1} and L_{aux1} [27]-[28].

However, at large current operation, the commutation time when the current flows from the bypass diode $D_{2,4}$ to the main diode $D_{1,3}$ is longer and recovery phenomenon might occur in the diode $D_{2,4}$ due to the stored charge in the bypass diode. Additionally, the reverse-recovery phenomenon is presented in the main diode.

Consequently, a novel ZCS interleaved boost converter, shown in Figure 3.16, is proposed. In this converter, the use of saturable inductors is introduced in order to reduce the reverse-recovery phenomenon and the EMI/RFI noises. In addition, the proposed converter can achieve a size reduction of the auxiliary inductors in comparison to the conventional topology.

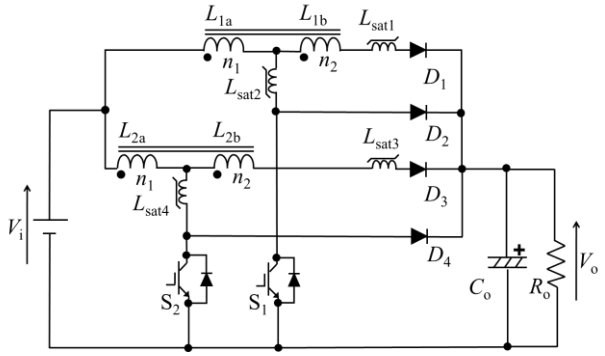
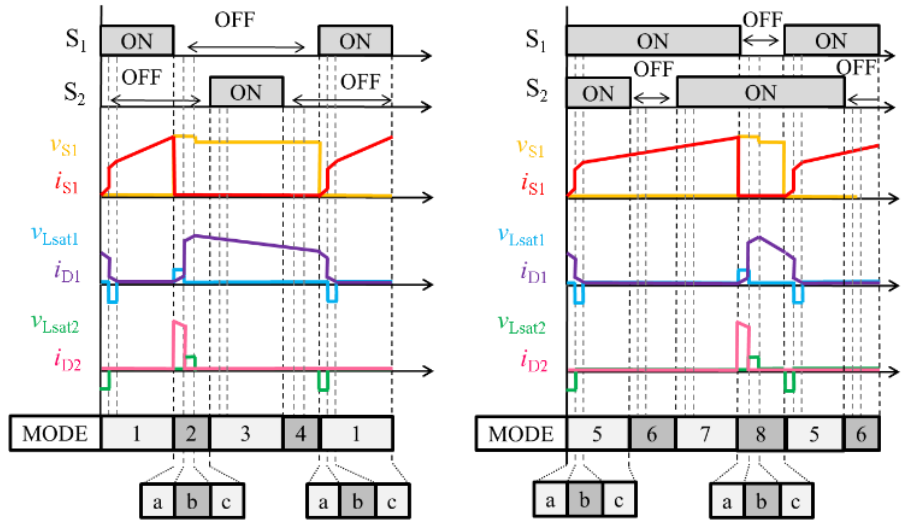


Figure 3.16. Proposed interleaved ZCS boost converter.

Figure 3.16 shows the proposed ZCS interleaved boost converter with saturable inductors. It is a two-phase boost converter constructed with two tapped inductors L_1 and L_2, where each inductor is made of two windings a and b, two main diodes D_1 and D_3, two bypass diodes D_2 and D_4, two power switches S_1 and S_2, that are switched with a 180-degree phase shift, a smoothing capacitor C_o and four particular auxiliary inductors L_{sat1}-L_{sat4}.These inductors operate as saturable inductors in order to achieve the reverse-recovery reduction and the ZCS behavior.

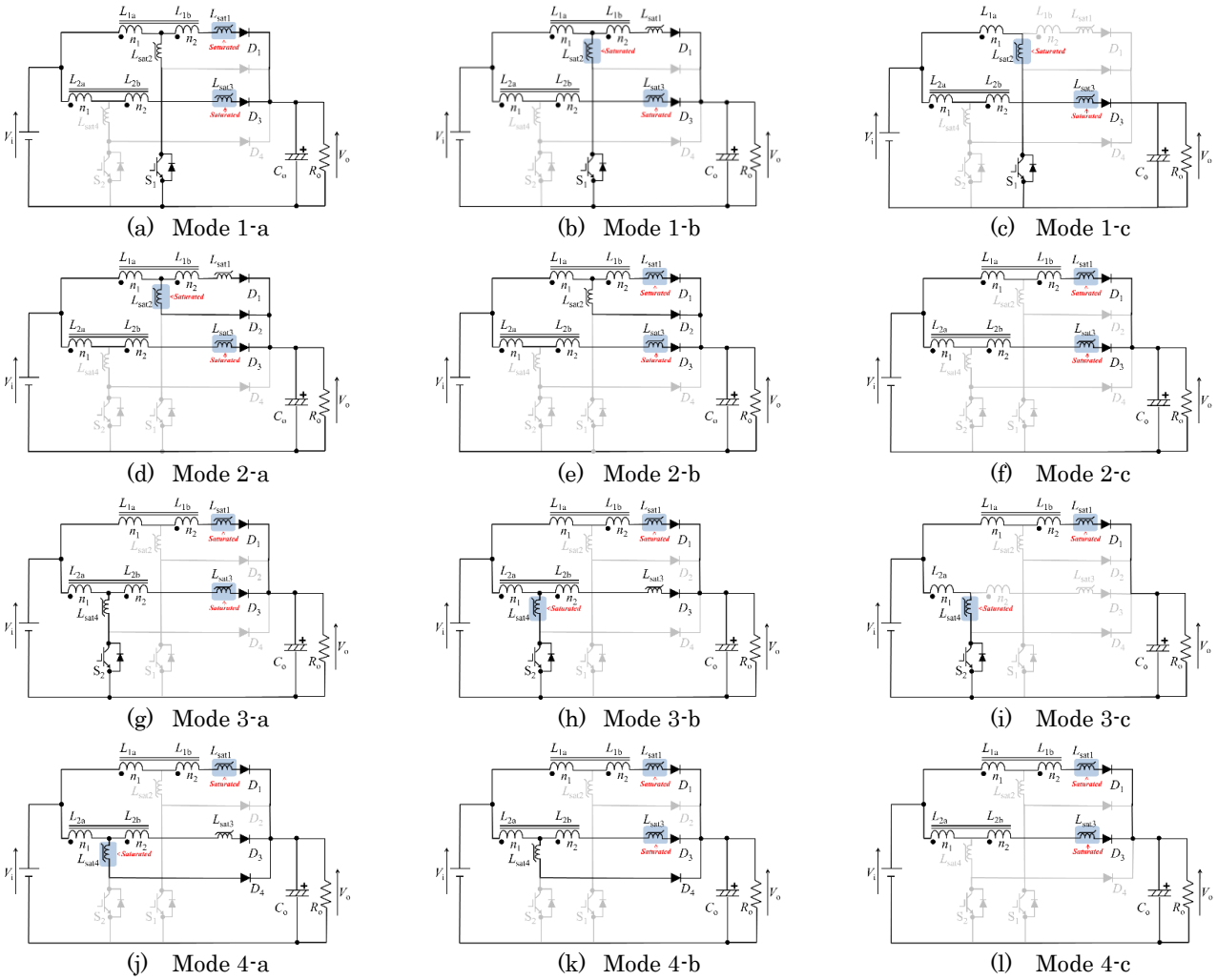
3.4.1 Operating Principle

Similarly to the operating principle of the single-phase recovery-less converter, the novel ZCS interleaved boost converter with saturable inductors has 24 operating modes that can be reduced into eight main modes where the commutation process is included. Therefore, as Figure 3.17 shows, when the proposed converter operates at a duty cycle lower than 50%, Modes 1-4 are presented and Modes 5-8 occur when the duty cycle is higher than 50%. Each mode has sub-modes a, b and c corresponding to the turning process. Figure 3.18 and Figure 3.19 show the operating modes when the converter is operating at a duty cycle of $D<0.5$ and $D>0.5$, respectively.



(a) D<0.5 (b) D>0.5

Figure 3.17. Operating waveforms.



(a) Mode 1-a (b) Mode 1-b (c) Mode 1-c

(d) Mode 2-a (e) Mode 2-b (f) Mode 2-c

(g) Mode 3-a (h) Mode 3-b (i) Mode 3-c

(j) Mode 4-a (k) Mode 4-b (l) Mode 4-c

Figure 3.18. Operating modes when D<0.5.

Mode 1: As Figure 3.18(a)-(c) show, S_1 is turned ON and S_2 remains OFF from its previous mode (Mode 4). Therefore, Sub-Modes 1a to1c occur.

Sub-Mode 1a, see Figure 3.18(a), occurs immediately after S_1 is turned ON while S_2 remains OFF. When S_1 is turned ON, the input current is divided between the main loop of the tapped inductor L_2, L_{sat3} and D_3, and the two loops of L_1. Consequently, the current through S_1 starts to increase slowly as the current through L_{1b}, L_{sat1} and D_1 starts to decrease while L_{sat1} remains under saturation (product of the previous state, Sub-Mode 4c).

Sub-Mode 1b, see Figure 3.18(b), is presented when the current of L_{sat1} decreases until the point where L_{sat1} is not anymore saturated and L_{sat2} goes into saturation. Consequently, there is a rapid response where the majority of L_{1a} current flows ascendant through L_{sat2} and S_1 as the current through L_{sat1} and D_1 decreases.

Finally, Sub-Mode 1c, see Figure 3.18(c), occurs when all L_{1a} current flows through L_{sat2} and S_1 while L_{sat2} is saturated and there is no more current through L_{1b}, L_{sat1} and D_1.

As a matter of fact, Sub-Modes 1a and 1b corresponds to the short process of turning ON that is the transition to the Sub-Mode 1c. This commutation process is repetitive in the operating principle of this converter, therefore, in order to summarize, this process will be cited.

Mode 2: Based on Figure 3.18(d)-(f), S_1 is turned OFF, S_2 remains OFF and Sub-Modes 2a to 2c occur.

Sub-Mode 2a, see Figure 3.18(d), occurs immediately after S_1 is turned OFF while S_2 remains OFF. This sub-mode corresponds to the short transition period when the S_1 is turned OFF and L_{1a} current is divided between the main loop of L_{1b}, L_{sat1} and D_1, and the bypass loop of L_{sat2} and D_2. Consequently, as L_{sat2} remains in saturation the majority of current flows through the bypass loop and starts to decrease as the current through the main loop starts to increase from zero. Moreover, the state of the main loop of L_2 remains the same as the previous mode.

Sub-Mode 2b, see Figure 3.18(e), is presented when the current through L_{sat2} is decreased until the point when L_{sat2} is not anymore in saturation, then the majority of L_{1a} current flows through L_{1b}, L_{sat1} and D_1, consequently L_{sat1} is saturated. The current through the main loop is increased until the current through the bypass loop becomes zero.

And, Sub-Mode 2c, see Figure 3.18(f), is presented when the bypass current of D_2 becomes zero, then the input current is completely divided between both main loops, though L_1 and L_2.

In fact, Sub-Modes 2a and 2b correspond to the short process of turning OFF that gives the transition to Sub-Mode 2c. As Mode 1, the turning OFF commutation process is also repetitive in the operating principle of this converter, therefore, this process will be cited during the next modes.

Mode 3: Considering Figure 3.18(g)-(i), where S_2 is turned ON and S_1 remains OFF, it is possible to infer that Mode 3 is the dual of Mode 1.

Then, Sub-Modes 3a and 3b, see Figure 3.18(g) and (h), correspond to the turning ON commutation process of S_2 where L_{sat3} and L_{sat4} are saturated alternatively as it was explained in Sub-Modes 1a and 1b.

Finally, in Sub-Mode 3c, see Figure 3.18(i), the input current is divided between the main loop of L_1, L_{sat1}, D_1 and C_o and the loop of L_{2a}, L_{sat4} and S_2. L_{sat1} and L_{sat4} remain in saturation.

Mode 4: As Figure 3.18(j)-(l) show, S_2 is turned OFF while S_1 remains OFF, consequently Mode 4 is the dual of Mode 2.

Therefore, Sub-Modes 4a and 4b, see Figure 3.18(j) and (k), correspond to the turning OFF commutation process of S_2 where L_{sat3} and L_{sat4} are alternatively saturated as it was explained in Sub-Modes 2a and 2b.

And, Sub-Mode 4c, see Figure 3.18(l), exhibits the same behavior as Sub-Mode 2c. Finally, it is important to highlight that Mode 1 occurs after Mode 4 when the converter is operating at a duty cycle lower than 50%.

Mode 5: For the case when the converter is under operation of a duty cycle higher than 50%, and based on Figure 3.19(a)-(c), S_1 is turned ON and S_2 remains ON from the previous mode (Sub-Mode 8c). In Mode 5, Sub-Modes 5a to 5c are presented.

Sub-Mode 5a, as Figure 3.19(a) shows, occurs when S_1 is turned ON and the input current is divided between the loop of L_2, L_{sat4} and S_2, and the two loops of L_1. Consequently, the behavior of L_{1a} current is the same as the L_{1a} current of Sub-Mode 1a explained above where the current through the main diode D_1 decreases as the current through S_1 increases. See Mode 1 operation.

Then, for Sub-Mode 5b, as Figure 3.19(b) shows, L_{2a} current still flows through S_2 and L_{sat4} while L_{sat1} goes out of saturation and the transition current is presented, therefore L_{sat2} is saturated and the current through S_1 increases as D_1 current decreases. The operation of this transition is the same as the explained in Sub-Mode 1b for L_{sat1} and L_{sat2}.

Finally, Sub-Mode 5c, as Figure 3.19(c) shows, corresponds to the mode where the current through D_1 becomes zero and therefore all L_{1a} current flows through S_1 while L_{2a} current flows through S_2. Moreover, L_{sat2} and L_{sat4} are saturated.

Mode 6: As Figure 3.19(d)-(f) show, S_2 is turned OFF, S_1 remains ON, and Sub-Modes 6a to 6c are presented.

Sub-Mode 6a, as Figure 3.19(d) shows, occurs immediately after S_2 is turned OFF and the majority of L_{2a} current starts to flow descendant though L_{sat4} (saturated) and D_4 while the current through D_3 starts to increase from zero. In fact, the behavior of L_{2a} current is the same as the L_{2a} current of Mode 4a explained above. In addition, L_{1a} current still flows through L_{sat2} and S_1.

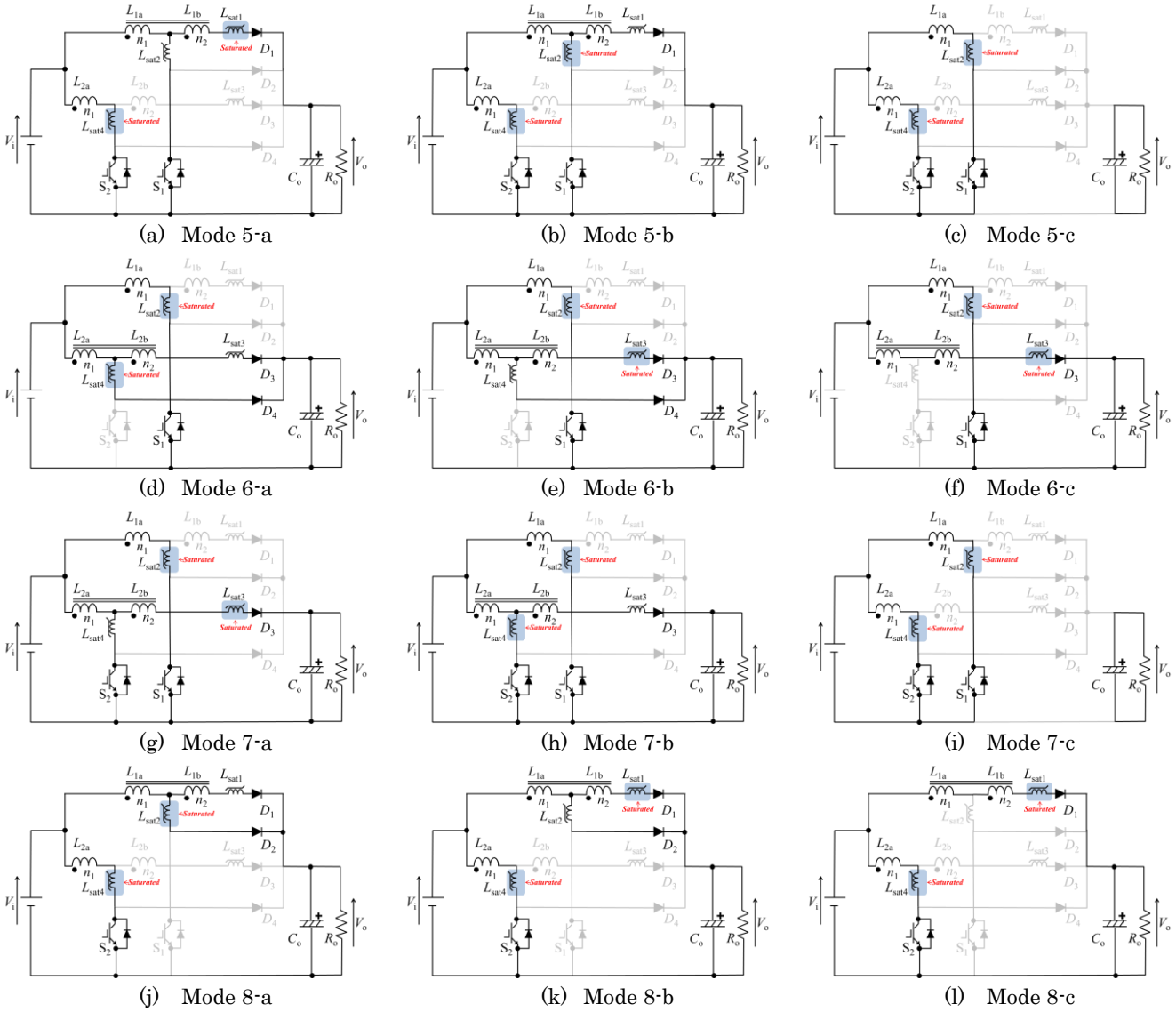


Figure 3.19. Operating modes when D>0.5.

Sub-Mode 6b, as Figure 3.19(e) shows, is presented when L_{sat4} goes out of saturation and the transition current occurs while L_{1a} current remains flowing through L_{sat2} and S_1. Therefore, L_{sat3} is saturated and the majority of L_{2a} current increases through L_{sat3} and D_3, while the current through L_{sat4} and D_4 is decreased. The operation of this transition is the same as the explained in Sub-Mode 4b for L_{sat3} and L_{sat4}.

Finally, Sub-Mode 6c, as Figure 3.19(c) shows, corresponds to the mode where the current through L_{sat4} and D_4 becomes zero and therefore all L_{2a} current flows through L_{sat3} and D_3 while L_{1a} current flows through S_1. L_{sat2} and L_{sat3} are saturated. This sub-mode has the same operation of Sub-Mode 1c.

Mode 7: Considering Figure 3.19(g)-(i), where S_2 is turned ON and S_1 remains ON, it is possible to infer that Mode 7 is the dual of Mode 5.

Consequently, Sub-Modes 7a and 7b, as Figure 3.19(g) and (h) show, correspond to the turning ON commutation process of S_2 where L_{sat3} and L_{sat4} are alternatively saturated as it was explained in Sub-Modes 3a and 3b for L_{sat3} and L_{sat4} or in Sub-Modes 5a and 5b for L_{sat1} and L_{sat2}.

Finally, in Sub-Mode 7c, as Figure 3.19(i) shows, the input current is divided between the loop of L_{1a}, L_{sat2} and S_1 and the loop of L_{2a}, L_{sat4} and S_2. L_{sat2} and L_{sat4} remain in saturation.

Mode 8: As Figure 3.19(j)-(l) show, S_1 is turned OFF while S_1 remains ON, therefore, it is possible to conclude that Mode 8 is the dual of Mode 6.

Consequently, Sub-Modes 8a and 8b, as Figure 3.19(j) and (k) show, correspond to the turning OFF commutation process of S_1 where L_{sat1} and L_{sat2} are alternatively saturated as it was explained in Sub-Modes 2a and 2b for L_{sat1} and L_{sat2} or in Sub-Modes 6a and 6b for L_{sat3} and L_{sat4}.

Then, Sub-Mode 8c, as Figure 3.19(l) shows, occurs when the current through D_2 becomes zero and therefore the input current is divided between the loop of L_{2a}, L_{sat4} and S_2 and the main loop of L_1, L_{sat1}, D_1 and C_o. This sub-mode exhibits the same behavior as Sub-Mode 3c.

Finally, it is important to mention that Mode 5 is presented after Mode 8 when the converter is operating at a duty cycle higher than 50%.

3.4.2 Suppression of the recovery phenomenon and ZSC behavior

- ***Reverse-Recovery Reduction***

Figure 3.20 shows the commutation current in the main Diodes D_1 and D_3 and in the bypass Diodes D_2 and D_4. There are two transition processes, one corresponds to the short transition immediately after S_1 or S_2 are turned ON and the other after S_1or S_2 are turned OFF.

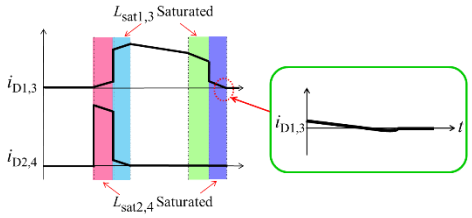


Figure 3.20. Diodes commutation current in the proposed converter.

Therefore, as it was explained above, these commutation processes occur because of the effect of the saturable inductors. Consequently, when the switch is turned ON the majority of the input current still flows through the main diode $D_{1,3}$ while $L_{sat1,3}$ remains saturated. Then, the main diode current decreases until the point where $L_{sat1,3}$ goes out of saturation

and the transition occurs. The majority of the input current flows through the switch $S_{1,2}$ while the main diode current decreases to zero.

As a consequence of this transition process, the commutation duration is decreased and the slope of the main and bypass diode currents are reduced in comparison to the conventional ZCS interleaved converter, see Figure 3.21.

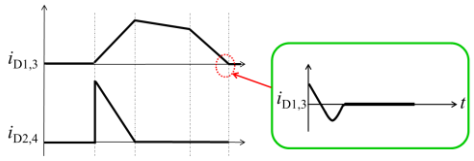


Figure 3.21. Diodes commutation current in the conventional converter.

Finally, as the slope is smaller, the recovery current is considerable reduced and therefore the switching losses produced by the reverse-recovery phenomenon are reduced as well.

- ***ZCS Behavior***

As Figure 3.22 shows, the proposed converter presents ZCS due to the presence of the saturable inductors and the commutation process that they produce.

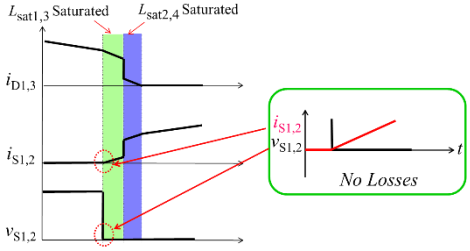


Figure 3.22. Switch commutation process in the proposed converter.

Therefore, as it was explained before, immediately after the switch is turned ON the main diode current starts to decrease softly due to the presence of stored energy in the saturable inductor $L_{sat1,3}$. In addition, the switch current starts to increase softly from zero because of the effect of the saturable inductor $L_{sat2,4}$ that avoid a large slope of the switch current.

As a consequence of this process, switching losses produced by the turning-on process in the switches are minimized.

3.4.3 Experimental validation

In order to have an experimental validation of the effectiveness of the proposed ZCS interleaved converter with saturable inductors, a 600W prototype was constructed and experimentally tested. Additionally, a 600W prototype of the conventional ZCS interleaved converter with auxiliary inductors was constructed with the purpose of comparing the

recovery phenomenon and the size reduction. Table 3.2 and Figure 3.23 show the circuit parameters and a photo of the experimental setup.

Table 3.2 Design Parameters of the Conventional and ZCS Interleaved Converter

Parameter		Conventional	Two-phase ZCS
Input voltage [V]	V_i	100	100
Output voltage [V]	V_o	200	200
Tapped inductor [μH]	L_1	650	650
Tapped inductor [μH]	L_2	660	660
Auxiliary inductor [μH]	L_{aux1}	22.6	--
Auxiliary inductor [μH]	L_{aux2}	23.8	--
Saturable inductor [μH]	L_{sat1}	--	19.1
Saturable inductor [μH]	L_{sat2}	--	18.7
Saturable inductor [μH]	L_{sat3}	--	18.3
Saturable inductor [μH]	L_{sat4}	--	18.2
Switching frequency [kHz]	f_s	50	50
Output capacitance [μF]	C_o	60	60
Turns ratio	n_1:n_2	5:1	5:1

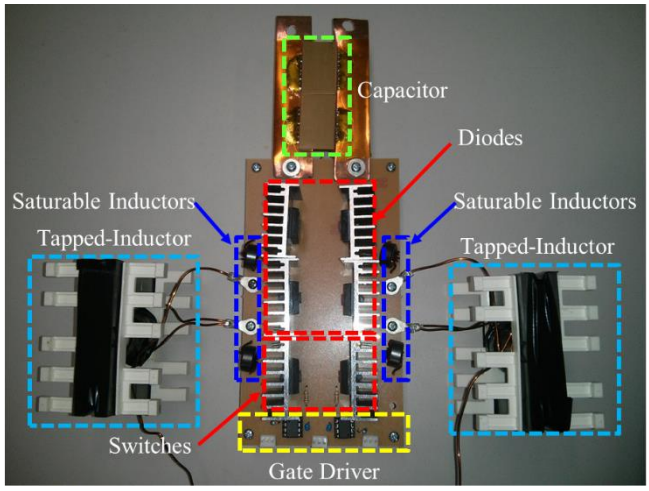


Figure 3.23. Experimental setup.

These prototypes were constructed with 600V Mosfets, 600V Silicon Diodes, Ferrite cores and Multilayered Ceramic Capacitors. As a matter of fact, these capacitors were selected due to their small resistance (1mΩ) and the advantage of the interleaved technique that allows the downsizing of output capacitors because higher frequency operation is presented [29]-[32]. Figure 3.24 shows the interleaving waveforms of the proposed converter.

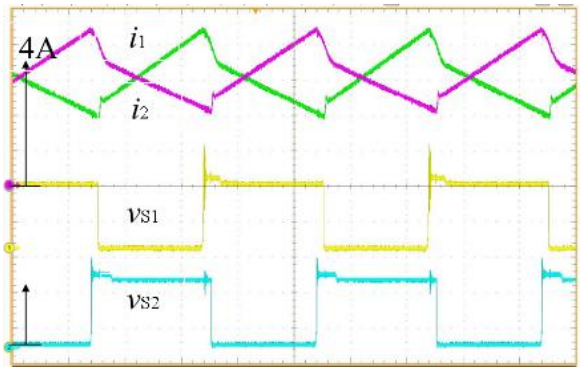


Figure 3.24. Switches voltages vs. input currents in the proposed converter.

- ***Size Comparison***

Figure 3.25 shows the size comparison of the two auxiliary inductors used in the prototype of the conventional ZCS interleaved converter and the four saturable inductors used in the proposed converter.

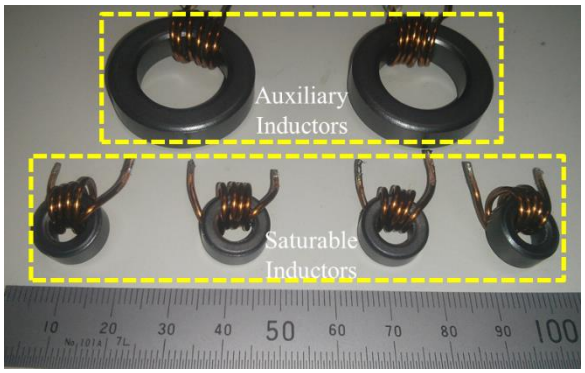
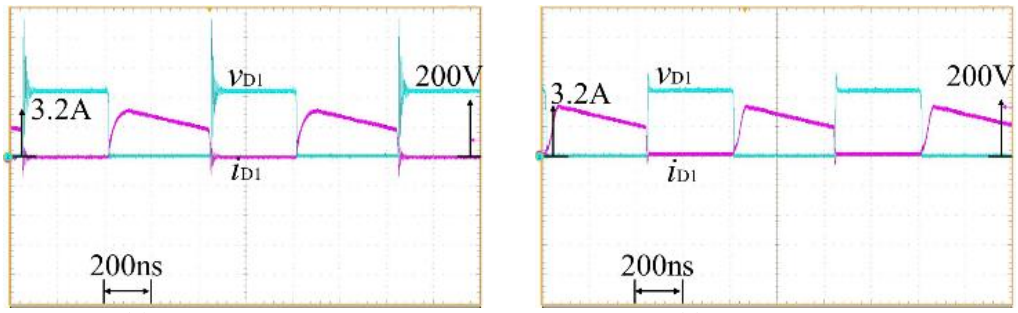


Figure 3.25. Inductor size comparison.

As a result, the auxiliary inductors used in the conventional converter have a cross sectional area of 0.48 cm^2, while the saturable inductors of the proposed circuit have a cross sectional area of 0.23 cm^2. Therefore, a total volume of the two auxiliary inductors was 7.78 *cc* compared to the 2.84 *cc* of the four saturable inductors. Conclusively, the proposed converter presents a reduction of 63.5% in the size of the auxiliary inductors even when the proposed converter used two additional inductors in comparison to the conventional circuit.

- ***Comparison of the Reverse-Recovery Reduction***

Figure 3.26 shows the comparison of the main diode current and voltage. Therefore, it is possible to conclude that the proposed converter offers a reduction of the surge voltage in the main diode because the presence of the saturable inductor in the main loop produces a damped effect in the diode voltage due to the resonance of the inductance L_{sat2} and the internal capacitance of the diode.

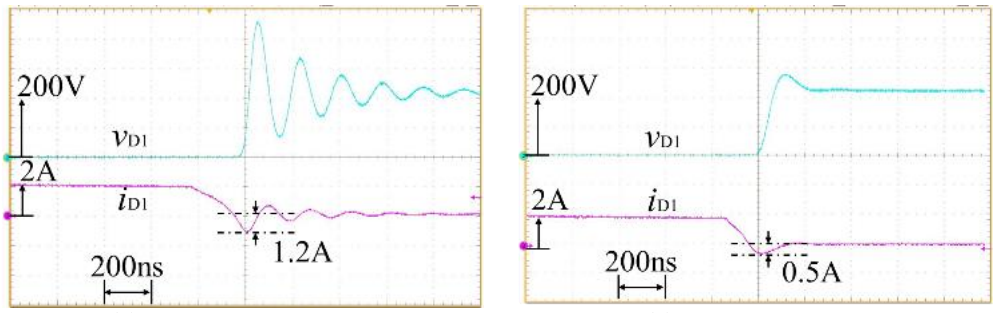


(a) Conventional circuit (b) Proposed circuit

Figure 3.26. Voltage and current waveforms of the main diode D_1.

Moreover, Figure 3.26 shows the difference between the diode current when the switch is turned OFF where the proposed converter has a shorter transition.

Additionally, Figure 3.27 shows the comparison of the reverse-recovery reduction. Therefore, the propose converter has a reverse-recovery current of 0.5A while the conventional circuit presents 1.2A. It means, a reduction of 58% in the reverse-recovery current. Finally, Figure 3.27 shows the advantage of the proposed converter in surge reduction of the diode voltage.

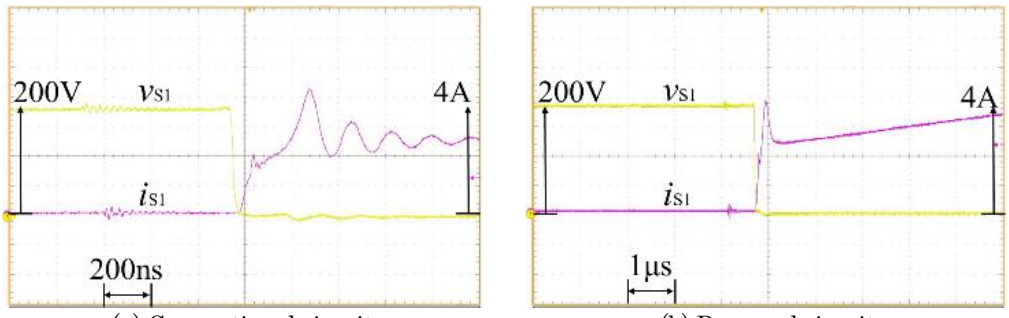


(a) Conventional circuit (b) Proposed circuit

Figure 3.27. Reduction of recovery phenomenon in the main diode D_1.

- ***Comparison of the ZCS Behavior***

Finally, the ZCS behavior was analyzed. Figure 3.28 shows the switch current and the voltage waveforms when the switch is turned ON. Consequently, it is possible to affirm that both topologies present ZCS behavior because in both circuits the drain-source voltage becomes zero while the current does not start to increase. However, it is evident the noise reduction in the current waveform of the proposed converter due to the presence of the saturable inductors.



(a) Conventional circuit (b) Proposed circuit

Figure 3.28. Turning ON process of the switch S_1.

3.5 Conclusions

A novel single-phase recovery-less boost converter with saturable inductors was proposed in this section. First, the circuit configuration, the operating principle and the disadvantages of the conventional recovery-less converter with auxiliary inductor were introduced. Then, the operating principle and the operation of the reverse-recovery reduction of the proposed converter were analyzed. Then, the design procedure of the saturable inductors was presented. Finally, a performance comparison was conducted from the experimental point of view. Prototypes of the conventional and the proposed converter were evaluated. From these tests, it was confirmed the effectiveness of the proposed converter in the suppression of the recovery phenomenon, with a 72% of reduction. Additionally, the downsizing advantage of the proposed converter was illustrated, where it was possible to see that the conventional topology needs an inductor with larger dimension in comparison with the two saturable inductors of the proposed converter. Therefore, a reduction of 63.5% in the core volume was achieved. Finally, efficiency tests were conducted and an increase of 1.2% of the total efficiency in the proposed converter was obtained.

Additionally, the two-phase interleaved topology was introduced as well. The circuit configuration and the operating principle were presented. In addition, the recovery phenomenon and the switching behavior were analyzed. Finally, a performance comparison was conducted from the experimental point of view. Prototypes of the conventional and the presented two-phase converter were evaluated. From these tests, the effectiveness of the proposed converter in the suppression of the recovery phenomenon, with a reduction of a 58% in the recovery current, was confirmed. Additionally, the downsizing advantage of the proposed converter was illustrated, where the conventional topology needs auxiliary inductors with bigger size in comparison to the four saturable inductors of the proposed converter. Specifically, a reduction of 63.5% in the auxiliary inductors size was achieved.

Based on the validation of the advantages of the proposed converters (single-phase and two-phase interleaved) in terms of core downsizing, reverse-recovery reduction and ZCS

operation, it is possible to conclude that it is a promising topology for vehicular applications where high power density and high efficiency are required.

References

[1] F. Guedon, S. Singh, R. McMahon and F. Udrea, "Boost Converter with SiC JFETs: Comparison with CoolMOS and Tests at Elevated Case Temperature," *IEEE Transactions on Power Electronics*, vol.28, no.4, pp.1938-1945, 2013.

[2] Toyota Motor Corporation, "Toyota PriusV Hybrid Vehicle Dismantling Manual," pp. 1-30, 2011.

[3] W. Li and X. He, "ZVT interleaved boost converters for high-efficiency, high step-up DC-DC conversion," *IET Trans. Power Electron.*, vol. 1, no. 2, pp. 284–290, 2007.

[4] R. Wai, C. Lin, R. Duan and Y. Chang, "High-efficiency DC–DC converter with high voltage-gain and reduced switch stress," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 354–364, 2007.

[5] R. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," 2nd ed. Norwell, MA: Kluwer, 2001.

[6] Y. Zhao; W. Li and X. He, "Single-Phase Improved Active Clamp Coupled-Inductor-Based Converter with Extended Voltage Doubler Cell," *IEEE Transactions on Power Electronics,* vol.27, no.6, pp.2869-2878, 2012.

[7] S. Dwari and L. Parsa, "An Efficient High-Step-Up Interleaved DC–DC Converter with a Common Active Clamp," *IEEE Transactions on Power Electronics*, vol.26, no.1, pp.66-78, 2011.

[8] Z. Shi, K. Cheng, and S. Ho, "Static performance and parasitic analysis of tapped-inductor converters," *IET Power Electronics*, Vol.7, no.2, pp.366-375, 2014.

[9] W. Martinez and C. Cortes, "High Power Density Interleaved DC-DC Converter for a High Performance Electric Vehicle," *IEEE Workshop on Power Electronics and Power Quality – PEPQ*A, pp. 1-6. 2013.

[10] W. Martinez and C. Cortes, "Design a DC-DC Converter for a High Performance Electric Vehicle," *IEEE International Conference on Connected Vehicles and Expo – ICCVE*, pp. 335-340, 2012.

[11] N. Ramos, M. Escoto and C. Odulio, "Design and analysis of an interleaved tapped-inductor boost converter for higher power and voltage-gain applications," *IEEE Region 10 Conference TENCON 2012*, pp.1-6, 2012.

[12] M. Gitau, F. Mukundi and W. Hofsajer, "Analysis and Design of a Single-Phase Tapped- Coupled-Inductor Boost DC-DC Converter," *Journal of Power Electronics,* Vol. 13, No. 4, pp. 636-646, 2013.

[13] K. Imai, T. Kawashima, S. Funabiki, M. Yamamoto and M. Tsuruya, "High Efficiency Low Noise SMPS System - Single Phase PFC Rectifier Side," *Power Conversion Conference - Nagoya, PCC '07*, pp.377-383, 2007.

[14] T. Kawashima, S. Funabiki, M. Yamamoto, M. Tsuruya and M. Ochiai, "Recovery-less Boost Converter for Electric Vehicle," *Journal of the Japan Institute of Power Electronics*, Vol. 33, pp.107-114, 2008.

[15] T. Kawashima, S. Funabiki, and M. Yamamoto, "Recovery-less boost converter for electric vehicle," *Proc. European Conf. on Power Electron. and Applicat. EPE-09.*, pp. 1-10, 2009.

[16] J. Kwon, W. Choi, and B. Kwon, "Cost-Effective Boost Converter with Reverse-Recovery Reduction and Power Factor Correction," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, pp. 471-473, 2008.

[17] W. Martinez, M. Yamamoto, P. Grbovic and C. Cortes, "Efficiency Optimization of a Single-Phase Boost DC-DC Converter for Electric Vehicle Applications," *IEEE 40th Annual Conference of the IEEE Industrial Electronics Society – IECON*, pp. 1-6, 2014.

[18] M. Yamamoto, H. Toda, T. Kawashima and T. Yoshida, "Hybrid Recovery-less Method Soft Switching Boost Chopper Circuit," *IEEJ Transactions on Industry Applications*, Vol.131, No. 9, pp.1171-1172, 2011.

[19] K. Nanamori, K. Kono, J. Imaoka, H. Tsukamoto and M. Yamamoto, "Verification of novel recovery-less boost converter with saturable inductor," *International Conference on Renewable Energy Research and Applications (ICRERA)*, pp.1-3, 2012.

[20] G. Joung, K. Ma and Y. Kim, "Battery discharger applications of high frequency boost converter with lossless snubber," *Power Electronics Specialists Conference,* pp. 938-942, 2002.

[21] J. Imaoka, S. Kimura, W. Martinez and M. Yamamoto, "A Novel Integrated Magnetic Core Structure Suitable for Transformer-linked Interleaved Boost Chopper Circuit," *IEEJ Journal of Industrial Applications*, vol.3, no.5, pp.395-404, 2014.

[22] N. Ramos, M. Escoto C. Odulio, "Design and analysis of an interleaved tapped-inductor boost converter for higher power and voltage-gain applications," *IEEE Region 10 Conference TENCON 2012*, pp.1-6, 2012.

[23] Z. Shi, K. Cheng, and S. Ho, "Static performance and parasitic analysis of tapped-inductor converters," *IET Power Electronics*, Vol.7, no.2, pp.366-375, 2014.

[24] K. Nanamori, K. Kono, J. Imaoka, H. Tsukamoto and M. Yamamoto, "Verification of novel recovery-less boost converter with saturable inductor," *International Conference on Renewable Energy Research and Applications (ICRERA)*, pp.1-3, 2012.

[25] T. Kawashima, S. Funabiki, M. Yamamoto, M. Tsuruya and M. Ochiai, "Recovery-less Boost Converter for Electric Vehicle," *Journal of the Japan Institute of Power Electronics*, Vol. 33, pp.107-114, 2008.

[26] T. Kawashima, S. Funabiki, and M. Yamamoto, "Recovery-less Boost Converter for Electric Vehicle," *Proc. European Conf. on Power Electron. and Applicat. EPE-09.*, pp. 1-10, 2009.

[27] M. Yamamoto, H. Toda, T. Kawashima and T. Yoshida, "Hybrid Recovery-less Method Soft Switching Boost Chopper Circuit," *IEEJ Trans. on Industry Applications*, Vol.131, No. 9, pp.1171-1172, 2011.

[28] J. Kwon, W. Choi, and B. Kwon, "Cost-Effective Boost Converter with Reverse-Recovery Reduction and Power Factor Correction," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, pp. 471-473. 2008.

[29] P. Wong, P. Xu, B. Yang and F. C. Lee, "Performance Improvements of Interleaving VRMs with Coupling Inductors," *IEEE Transactions on Power Electronics*, Vol.16, no.4, pp.499-507, 2001.

[30] K. Katsura and M. Yamamoto, "Optimal stability control method for transformer-linked three-phase boost chopper circuit," *IEEE Energy Conversion Congress and Exposition (ECCE),* pp. 1082-1087. 2012.

[31] W. Martinez, S. Kimura, J. Imaoka, M. Yamamoto, K. Umetani, S. Arimura and T. Hirano, "High Power Density DC-DC Converter for Home Energy Management Systems," *International Conference on Intelligent Green Building and Smart Grid (IGBSG)*, pp. 1-6, 2014.

[32] S. Dwari and L. Parsa, "An Efficient High-Step-Up Interleaved DC–DC Converter with a Common Active Clamp," *IEEE Transactions on Power Electronics*, vol.26, no.1, pp.66,78, 2011.

4. High Step-Down Converter

4.1 Introduction

High power density DC-DC converters have become important components in networking, telecommunications, and computing applications where the supply voltage is higher than the required by the load [1]-[5]. Moreover, digital equipment such as, *inter alia*, MCUs (Micro Controller Unit), FPGAs (Field Programmable Gate Array) and ASICs (Application Specific Integrated Circuit) on mother boards usually require a very low feeding voltage with the purpose of increasing the efficiency and the power consumption of these devices [6]-[7]. Therefore, step-down converters with a High Step-Down (HSD) conversion ratio have gained attention to interface the power supply with the digital equipment that requires a much lower voltage [8]-[10].

Nevertheless, conventional topologies present some drawbacks when a high step-down ratio is required. These drawbacks appear mainly by three reasons: 1) A very small duty cycle is required to achieve the required output voltage which produces extremely high losses in the components due to the parasitic effects; 2) Usually, conventional converters cannot achieve high step-down conversion ratio because of the presence of parasitic resistances, capacitances and inductances in the components; and 3) Conventional converters have low power density because they use bulky components to achieve the required voltage and current ripples [11]-[14]. Consequently, the demand of high step-down conversion techniques has gradually increased according to the downsizing and low-voltage requirements of digital equipment [15]-[17].

Currently, there are several step-down topologies with high conversion ratio performance. However, most of them present problems regarding low power density because they need many additional passive components to achieve a high conversion ratio. This study focuses on these problems and propose the use of interleaving phases and magnetic coupling, as they are well-known techniques to increase the power density and downsize magnetic components [18]-[20]. Interleaving phases is effective because the input current is divided into the number of phases. Therefore, a reduction in the power ratings of the components, as well as a size miniaturization of the capacitive components can be achieved as a result from the high frequency operation. Another aspect that makes magnetic coupling effective is the size reduction of the magnetic components it provides as a result of the integration of several windings into only one core. The magnetic coupling

technique may reduce the input current ripple of the converter as well [21]-[23]. In Figure 4.1 it is depicted the proposed high step-down interleaved converter with integrated coupled inductor that is proposed.

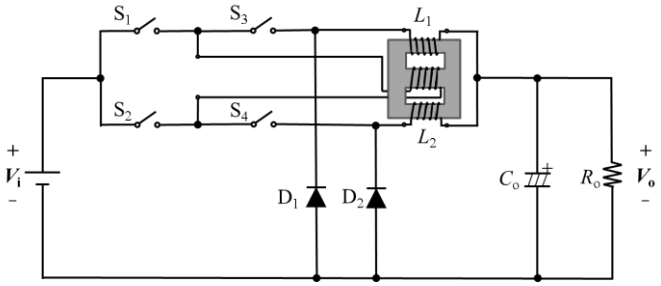


Figure 4.1. Proposed high step-down two-phase interleaved converter.

This section is organized as follows: First, the circuit configuration and the operating principle of the novel high step-down interleaved buck converter is presented with a particular integrated coupled-inductor that helps to tackle the problems described above. Second, the steady state analysis is conducted as the base to calculate the theoretical step-down conversion ratio of the proposed converter. Then, the performance of the proposed topology is compared with similar state of the art high step-down converters. Finally, experimental tests of several prototypes with different ratios of the number of turns are shown as a validation of the proposed topology.

4.2 High Step-Down Converter

The converter shown in Figure 4.1, is a two-phase interleaved buck converter made with a particular magnetic coupled-inductor constructed with three windings arranged in an EE core as shown in Figure 4.2.

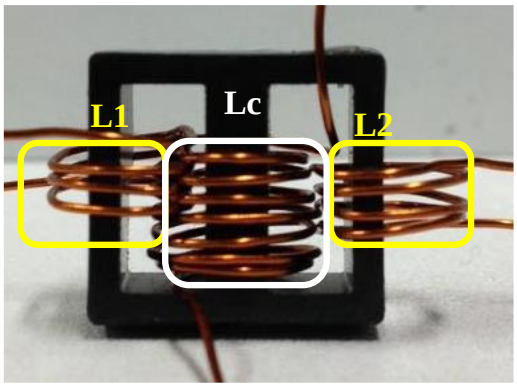


Figure 4.2. Coupled-inductor with 3 windings for a HSD converter.

The external windings are directly coupled and an air-gap is installed in each external leg to suppress DC flux induction. In addition, this converter has four power switches S_1-S_4 which are alternative commuted with a 180-degree phase shift between $S_{1,4}$ and $S_{2,3}$. In fact, each switch is driven by an independent gate drive circuit with isolated power supply.

Additionally, two diodes D_1 and D_2 are connected between the ground and the source of the switches S_3 and S_4, respectively, plus one output capacitor C_o. Each external winding, L_1 and L_2, is connected between the output capacitor and the cathodes of the diodes. Finally, the central winding L_c is located between the source terminals of S_1 and S_2. Consequently, compared to the conventional two-phase interleaved buck converter, the proposed topology has the addition of two switches and one winding [24].

The two-phase interleaved high step-down converter has four different operating modes corresponding to the combinations of the ON and OFF-states of the switches. Figure 4.3 shows the four operating modes and Figure 4.4 shows the operating waveforms of the proposed converter when it is operating under a Continuous Conduction Mode (CCM).

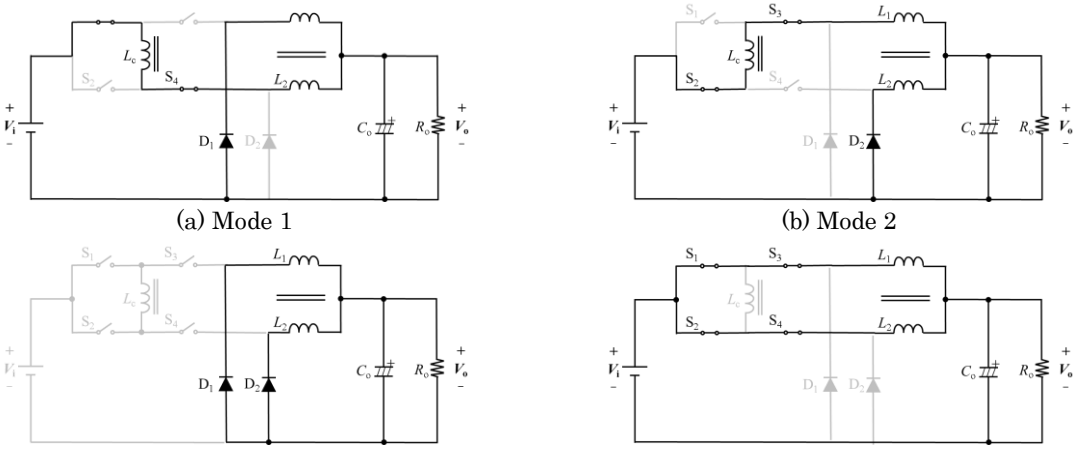


Figure 4.3. Operating modes of the HSD converter.

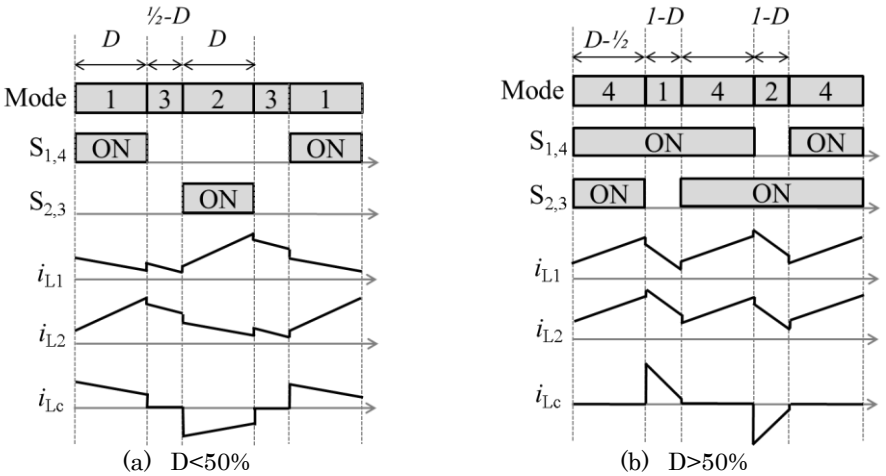


Figure 4.4. Operating waveforms.

Mode 1: As Figure 4.3(a) shows, during this interval, S_1 and S_4 are turned ON, while S_2 and S_3 are turned OFF. The input current increases linearly through the central winding L_c, the external winding L_2, the output capacitor and the load. In addition, there is a loop where the energy stored in the external winding L_1 is linearly discharged through the

output capacitor and the load across the diode D_1. In this mode, a positive voltage is induced in the central winding as a result of the voltage applied to the external windings.

Mode 2: Figure 4.3(b) shows Mode 2 as the dual of Mode 1 because S_1 and S_4 are turned OFF, while S_2 and S_3 are turned ON. The energy stored in the external winding L_2 is linearly discharged to the output capacitor and the load through the diode D_2. Thus, the input current increases linearly across the central winding L_c, where a negative voltage is induced because of the voltage applied to the external windings, the external winding L_1, the output capacitor and the load.

Mode 3: During this interval (see Figure 4.3(c)), all four switches S_1-S_4 are turned OFF. Therefore, there are only two discharging loops where the current generated by the external winding L_1 and L_2 decreases linearly across the output capacitor, the load and the diode D_1 and D_2, respectively. In this mode, the central winding does not affect the circuit behavior because no voltage is induced in the central winding.

Mode 4: Finally, as Figure 4.3(d) shows, during Mode 4, all four switches S_1-S_4 are turned ON. Consequently, the input current is divided into the winding currents flowing through L_1 and L_2. These currents join to flow through the output capacitor and the load. In this mode, as well as in Mode 3, there is no voltage induced in the central winding.

4.3 Analysis of the Step-Down Conversion Ratio

For analytical convenience in the steady state analysis and the post-deriving of the step-down conversion ratio expressions of the proposed converter, it is necessary to consider the induced voltage in each winding of the coupled-inductor. This deriving process is conducted based on the magnetic circuit of the integrated coupled inductor. Figure 4.5 shows the magnetic fluxes in the particular inductor.

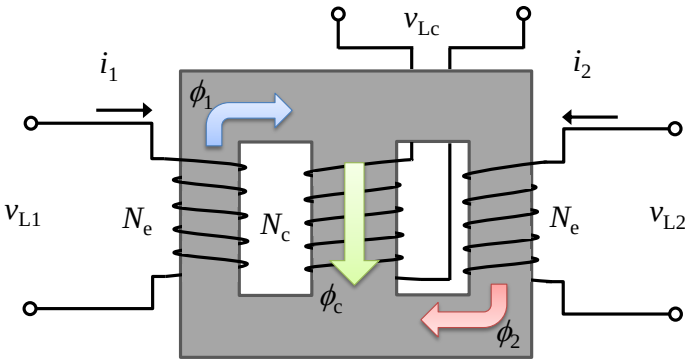


Figure 4.5. Magnetic fluxes in the coupled-inductor with 3 windings.

In this case, three magnetic fluxes circulate through in the core. These influence the induced voltages as follows:

$$v_{L1} = N_e \frac{d\phi_1}{dt} \tag{4.1}$$

$$v_{L2} = N_e \frac{d\phi_2}{dt} \tag{4.2}$$

$$v_{Lc} = N_c \frac{d\phi_c}{dt} \tag{4.3}$$

where, v_{L1}, v_{L2} and v_{Lc} are the external and central winding voltages, respectively; ϕ_1, ϕ_2 and ϕ_c are the external and central magnetic fluxes, respectively; and N_e and N_c the number of turns of the external and central winding, respectively. In addition, according to Figure 4.5, we obtain:

$$\phi_C = \phi_1 - \phi_2 \tag{4.4}$$

Consequently, from (4.1)-(4.4), the induced voltage in the central winding is produced by the applied voltage to the external windings L_1 and L_2 as follows:

$$v_{LC} = \frac{N_c(v_{L1} - v_{L2})}{N_e} \tag{4.5}$$

Hence, N is introduced as the ratio between the number of turns of the central and external windings:

$$N = \frac{N_c}{N_e} \tag{4.6}$$

Finally, from (4.5) and (4.6), it is possible to derive the induced voltage in the central winding accordingly with the introduced turns ratio N, as follows:

$$v_{LC} = N(v_{L1} - v_{L2}) \tag{4.7}$$

Using the voltage-second balance technique, the induced voltages in each external winding v_{L1} and v_{L2} are calculated in each operating mode, as it was described above. These derivations are conducted taking into account (4.7).

Mode 1:

$$v_{L1} = -v_o \tag{4.8}$$

$$v_{L2} = \frac{v_i - v_o(1+N)}{1+N} \tag{4.9}$$

Mode 2:

$$v_{L1} = \frac{v_i - v_o(1+N)}{1+N} \tag{4.10}$$

$$v_{L2} = -v_o \tag{4.11}$$

Mode 3:

$$v_{L1} = -v_o \tag{4.12}$$

$$v_{L2} = -v_o \tag{4.13}$$

Mode 4:

$$v_{L1} = v_i - v_o \tag{4.14}$$

$$v_{L2} = v_i - v_o \tag{4.15}$$

Equations (4.8)-(4.15) are helpful to derive the conversion ratio of the proposed converter.

Usually, two-phase interleaved topologies show two types of operational sequences: Sequence 1: Duty cycles lower than 50% and Stage 2: Duty cycles higher than 50%. Consequently, based on Figure 4.4, Sequence 1 presents Modes 1, 2 and 3, while Sequence 2 presents Modes 1, 2 and 4. Moreover, based on the steady-state analysis shown in the previous sub-section, the voltage conversion ratio for duty cycles D lower than 50% is derived from (4.8), (4.10) and (4.12) as follows:

$$M_{\mathrm{D<0.5}} = \frac{D}{1+N} \tag{4.16}$$

On the other hand, from (4.8), (4.10) and (4.14), the conversion ratio for the case when the duty cycle is higher than 50% is derived as:

$$M_{D>0.5} = \frac{D(1+2N)-N}{1+N} \tag{4.17}$$

As a result, when evaluating the ratio of the number of turns of *N=1*, *2* and *4*, and the conversion ratio of the conventional single-phase buck converter or the two-phase interleaved buck converter [24], it is possible to construct the ideal voltage according to the duty cycle as shown in Figure 4.6.

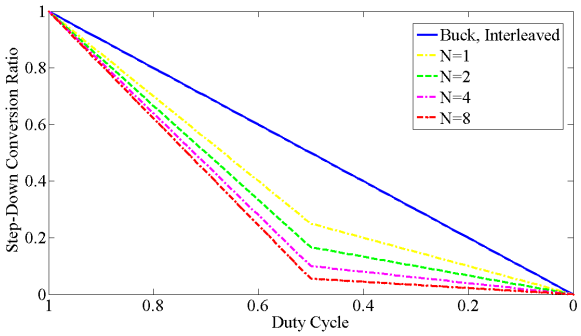


Figure 4.6. Conversion ratio comparison.

The step-down ratio of the buck converter is defined as:

$$M_{\text{buck}} = D \tag{4.18}$$

Summarizing, the proposed converter presents a high step-down ratio performance in comparison to the conventional single phase and two-phase interleaved buck converters.

4.4 Comparison with Conventional Topologies

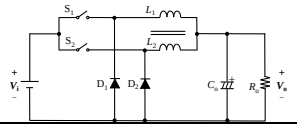
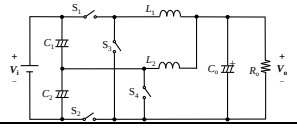
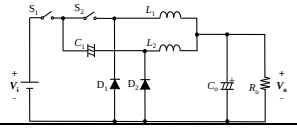
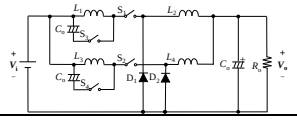
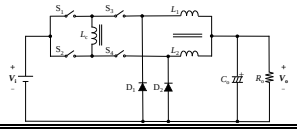
As it was mentioned above, two of the attractive features of the propose converter are the high step-down conversion ratio and the high power density that the topology can achieve due to its downsizing characteristics. Consequently, in this section, a performance comparison is shown with the purpose of making evident the effectiveness of the novel topology. Therefore, three outstanding high step-down topologies were selected from the literature in order to compare the number of components and their step-down ratio performances. The selection of the outstanding topologies, presented in [25]-[27], was conducted under the criteria of similarity of the interleaving phases and magnetic coupling techniques. Specially, the converter proposed in [27] has the similarity of the step-down ratio dependence on the turns ratio N of its coupled inductor

Consequently, Table 4.1 shows the characteristics comparison of the mentioned high step-down converters. In this table, the number of components and their step-down ratios are evaluated. In addition, Table 4.1 shows the characteristics of the conventional two-phase interleaved buck converter as well. Based on the comparison of Table 4.1, it is possible to conclude that the number of components of the proposed converter is comparable to the converters of [25] and [26], and it is less than the converter published in [27].

Moreover, the relationship between the step-down ratio and the duty cycle of the compared converters is shown in Figure 4.7. From Figure 4.7, it is possible to see the high step-down performance of the selected and the proposed topologies over the conventional buck converter. In addition, the converter reported in [25] offers a higher step-down conversion ratio than the other converters in duty cycles higher than 50%. On the other hand, in duty cycles lower than 50%, where the high step-down converters are more

required due to the high conversion ratio requirements, the proposed converter offers the highest step-down ratio in the comparison.

Table 4.1 HSD Converters Comparison

Converter	Configuration	Conversion Ratio	Sw	Di	Wins	Caps
Conventional Interleaved Buck		$M = D$	2	2	2	1
Converter published in [25]		$M = \frac{D}{2}$	4	0	2	3
Converter published in [26]		$M_{D<0.5} = \frac{D}{2}$ $M_{D>0.5} = D^2$	2	2	2	2
Converter published in [27]		$M = \frac{D}{D + N(1-D)}$	4	2	4	3
Proposed		$M_{D<0.5} = \frac{D}{1+N}$ $M_{D>0.5} = \frac{D(1+2N)-N}{1+N}$	4	2	3	1

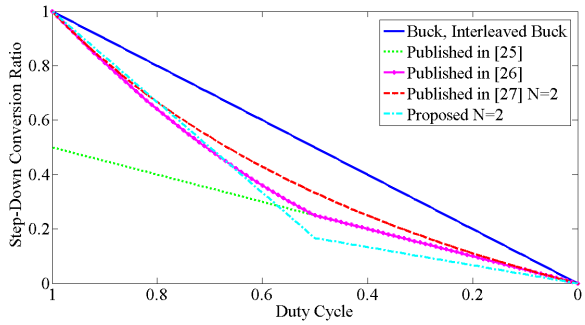


Figure 4.7. Step-down ratio of the proposed converter vs. other topologies.

Based on this comparison, it is possible to infer that the proposed converter theoretically offers a quite high step-down ratio in comparison to the number of components that requires.

4.5 Experimental Validation

With the purpose of validating and having a complete understanding of the effectiveness of the proposed high step-down converter, three prototypes were constructed and experimentally tested. These prototypes were tested to compare and evaluate the step-down conversion ratio of the proposed converter at different values of *N*. These circuits were constructed using 30V/5A Schottky Barrier Diodes, 30V/100A Power Mosfets,

Ceramic Capacitors and Ferrite Cores. Table 4.2 shows the experimental parameters of the tests.

Table 4.2 Experimental Parameters for HSD Evaluation

Parameters		Value
Input Voltage	V_i	1V – 20V
Output Voltage	V_o	1V
Output Load	R_o	3.9Ω
Duty Cycle	D	99% – 10%
Frequency	f	30kHz

These three circuits were experimentally tested with an open control loop programmable to 1V of output voltage, where the input voltage was varied between a range of 20V and 1V. These tests, were conducted with three different inductors made with different number of turns as Table 4.3 shows. Figure 4.8 shows the experimental setup of the proposed converter with *N=2.*

Table 4.3 Inductor Parameters for HSD Evaluation

		N=1	N=2	N=4
Number of turns	N	External: 4 turns Center: 4 turns	External: 4 turns Center: 8 turns	External: 4 turns Center: 16 turns
Inductance	L	L_1: 0.82 µH L_2: 0.85 µH L_c: 0.77 µH	L_1: 0.84 µH L_2: 0.85 µH L_c: 3.34 µH	L_1: 0.87 µH L_2: 0.89 µH L_c: 13.22 µH
ESR	R	R_1: 52 mΩ R_2: 53 mΩ R_c: 60 mΩ	R_1: 52 mΩ R_2: 53 mΩ R_c: 119 mΩ	R_1: 50 mΩ R_2: 51 mΩ R_c: 460 mΩ
Window area	A_w	34.3 mm²		
Sectional area	A_{core}	mm²		

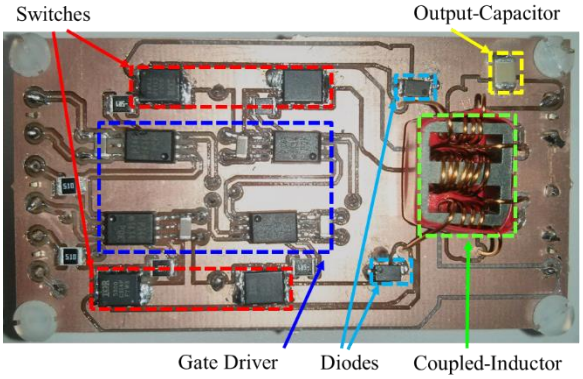


Figure 4.8. Prototype of the proposed high step-down converter.

Consequently, Figure 4.9 shows the experimental results of the three circuits in comparison to the conventional Buck converter. From this figure, it is possible to validate the effectiveness of the proposed high step-down two-phase interleaved boost converter with the particular coupled-inductor. It is evident the difference between the conversion ratios of the conventional interleaved converter and the proposed topology.

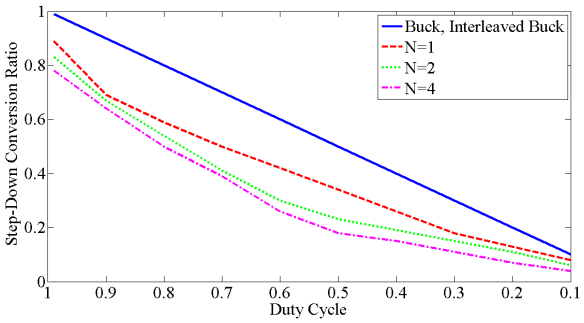


Figure 4.9. Experimental step-down conversion ratio.

As Figure 4.9 shows, the proposed converter is more effective at duty cycles lower than 50%. For example, the proposed converter with a turns ratio *N=2* achieves an increment of 40% in the step-down ratio when it is operating at a duty cycle of 30%. However, the experimental results present lower values in comparison to the theoretical calculation. This is because of the parasitic resistances and inductances presented in the coupled-inductor. Nevertheless, even with reduction generated by these parasitic components, the results revealed the effectiveness of the proposed converter in comparison to the ideal conventional topologies.

In addition, as it was explained before, these prototypes can manage a rated voltage of 30V and a rated current of 5A per phase. Therefore, the maximum allowable power of these prototypes is 300W. Moreover, taking into account the fact that the constructed prototype has a volume of 34.5 cc (including dead spaces, without casing), it is possible to mention that the maximum power density that this converter can manage is 8.7 W/cc.

4.6 Conclusions

A novel high step-down two-phase interleaved buck converter with a particular coupled-inductor was presented in this section. First, the circuit configuration and the operating principle were presented as the base of the steady-state analysis where it was possible to calculate the step-down ratio performance of the proposed converter. Then, a performance comparison of the presented converter with some outstanding high step-down converters was conducted. It was possible to see the effectiveness of the proposed topology over other topologies. Finally, some experimental tests were conducted as a validation of the theoretical calculations of the proposed converter. A power density of 8.7 W/cc was achieved. In addition, it was found that the proposed converter, when it is operating with a ratio of number of turns of 2 and a duty cycle of 30%, offers a step-down conversion ratio 40% bigger than the conventional interleaved buck converter.

Taking into account the advantages of this converter in terms of step-down ratio and power density, it is possible to conclude that it is a promising topology for networking, telecommunications and computing applications when a high conversion ratio is needed keeping a high power density.

References

[1] F. Lee and Q. Li, "High-Frequency Integrated Point-of-Load Converters: Overview," *IEEE Trans. on Power Electron.*, vol. 28, no.9, pp. 4127-4136, 2013.

[2] Q. Li, Y. Dong, F. Lee and D. Gilham, "High-Density Low-Profile Coupled Inductor Design for Integrated Point-of-Load Converters," *IEEE Trans. on Power Electron.*, vol. 28, no. 1, pp. 547-554, 2013.

[3] Y. Su, W. Zhang, Q. Li, F. Lee and M. Mu, "High Frequency Integrated Point of Load (POL) Module with PCB Embedded Inductor Substrate," In *Proc. IEEE Energy Conversion Cong. and Expo.*, *(ECCE2013)*, pp. 1243- 1250, 2013.

[4] J. Lee and B. Kwon, "DC–DC Converter Using a Multiple-Coupled Inductor for Low Output Voltages," *IEEE Trans. on Ind. Electron.*, vol. 54, no.1, pp. 467-478, 2007.

[5] A. De Nardo, M. Femia, G. Petrone and G. Spagnuolo, "Optimal Buck Converter Output Filter Design for Point of Load Applications," *IEEE Trans. on Ind. Electron.*, vol. 57, no.4, pp. 1330-1341, 2013.

[6] J. Imaoka, S. Kimura, W. Martinez and M. Yamamoto, "A Novel Integrated Magnetic Core Structure Suitable for Transformer-linked Interleaved Boost Chopper Circuit," *IEEJ Journal of Industry Applications*, vol.3, no.5, pp. 395-404, 2014.

[7] M. Pavlovsky, G. Guidi, and A. Kawamura, "Assessment of Coupled and Independent Phase Designs of Interleaved Multiphase Buck/Boost DC-DC Converter for EV Power Train," *IEEE Trans. on Power Electron.*, vol. 29, no. 6, pp. 2693-2704, 2013.

[8] P. Zumel, O. Garcia, J. A. Cobos and J. Uceda, "EMI Reduction by Interleaving of Power Converters," *IEEE Appl. Power Electron. Conf. and Expo. (APEC)*, vol. 2. pp.688-694, 2004.

[9] O. Machida, M. Yanagihara, E. Chino, S. Iwakami, N. Kaneko, H. Goto, and K. Ohtsuka, "Evaluation of reverse conduction GaN FETs," *Inst. Electron. Inf. Commun. Eng.*, vol. 108, no. 377, pp. 29–34, 2009.

[10] J. Delaine, P. Jeannin, D. Frey, K. Guepratte: "High Frequency DC-DC Converter Using GaN Device," *IEEE Appl. Power Electron. Conf. and Expo. (APEC)*, pp. 1754-1761. 2012.

[11] J. Imaoka, S. Kimura, Y. Itoh, M. Yamamoto, M Suzuki and K. Kawano, "Feasible evaluations of coupled multilayer chip inductor for POL converter," *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA)*, pp. 883-890, 2014.

[12] M. Hirakawa, M. Nagano, Y. Watanabe, K. Andoh, S. Nakatomi and S. Hashino, "High Power Density DC/DC Converter using the Close-Coupled Inductors," *1st IEEE Energy Conversion Congress and Exposition (ECCE),* pp.1760-1767. 2009.

[13] W. Martinez, J. Imaoka, S. Kimura, M. Yamamoto and C. Cortes, "Volume Comparison of DC-DC Converters for Electric Vehicles," *IEEE Workshop on Power Electronics and Power Quality Applications - PEPQA,* pp. 1-6, 2015.

[14] G. Calabrese, M. Granato, G. Frattini, and L. Caprineri, "Integrated Gate Drive Architecture for High Step-down Multiphase Buck Converter," *International Exhibition and Conference for Power Electronics PCIM Europe,* pp. 1-8, 2015.

[15] K. Tripetch, "A novel technique for step down converter implemented by high voltage operational amplifier," *International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM),* pp. 287-292, 2012.

[16] C. Yutian and L. Tolbert, "High step down ratio (400 V to 1 V) phase shift full bridge DC/DC converter for data center power supplies with GaN FETs," *IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA),* pp. 23-27, 2013.

[17] U. Masatoshi, "High Step-Down Converter Integrating Switched Capacitor Converter and PWM Synchronous Buck Converter," *35th International Telecommunications Energy Conference 'Smart Power and Efficiency' (INTELEC),* pp. 1-6, 2013.

[18] W. Martinez, J. Imaoka, Y. Itoh, M. Yamamoto and K. Umetani, "Analysis of Coupled-Inductor Configuration for an Interleaved High Step-Up Converter," *IEEE International Conference on Power Electronics – ICPE 2015-ECCE Asia,* pp. 2591-2598, 2015.

[19] W. Li, X. Xiang, C. Li, W. Li and X. He, "Interleaved High Step-Up ZVT Converter with Built-In Transformer Voltage Doubler Cell for Distributed PV Generation System," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 300-313. 2013.

[20] W. Martinez, M. Yamamoto, P. Grbovic and C. Cortes, "Efficiency Optimization of a Single-Phase Boost DC-DC Converter for Electric Vehicle Applications", *IEEE 40th Annual Conference of the IEEE Industrial Electronics Society – IECON*, pp. 4279-4285, Dallas-USA, Oct, 2014.

[21] R. Gules, L. Pfitscher and L. Franco, "An Interleaved Boost DC-DC Converter with Large Conversion Ratio," *IEEE International Symposium on Industrial Electronics, ISIE*, pp. 411-416, 2003.

[22] W. Martinez, S. Kimura, J. Imaoka, M. Yamamoto, K. Umetani, T. Hirano and S. Arimura, "High Power Density DC-DC Converter for Home Energy Management Systems", *IEEE International Green Building and Smart Grid Conference - IGBSG*, pp. 1-6, Taipei-Taiwan, April, 2014.

[23] R.J. Wai, C.Y. Lin, R.Y. Duan, and Y.R. Chang, "High Efficiency DC-DC Converter with High Voltage-gain and Reduced Switch Stress," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 354-364. 2007.

[24] M. Bendali, C. Larouci, T. Azib, C. Marchand and G. Coquery, "An Efficient High-Step-Up Interleaved DC–DC Converter with a Common Active Clamp," *IET Electrical Systems in Transportation*, vol.5, no. 1, pp. 53-60, 2015.

[25] C. Hsieh, T. Liang, L. Yuang, R. Lin and K. Chen, "Design methodology of an interleaved buck converter for onboard automotive application, multi-objective optimisation under multi-physic constraints," *IEEE Intern. Symp. on Circuits and Systems (ISCAS)*, pp.3697-3700, 2010.

[26] I. Lee, S. Cho and G. Moon, "Interleaved Buck Converter Having Low Switching Losses and Improved Step-Down Conversion Ratio," *IEEE Transactions on Power Electronics,* vol. 27, no. 8, pp. 3664-3675, 2012.

[27] C. Tsai and C. Shen, "A High Step-Down Interleaved Buck Converter with Active-Clamp Circuits for Wind Turbines," *Energies,* vol. 5, no. 12, pp. 5150-5170, 2012.

5. High Step-Up Interleaved Boost Converter

5.1 Introduction

Recently, High Step-Up (HSU) converters, identified as circuits capable of boosting the low voltage of a power supply to a much higher voltage, have gained great attention due to its potential in many applications [1]-[6]. These converters have found several industrial applications in Uninterruptible Power Systems (UPS) and some emergent communication systems. In addition, with the introduction of the renewable energies and their application in grid-connected systems, high step-up converters have been required to boost the low voltage of sustainable structures based on Photovoltaic (PV) or Fuel Cells [7]-[8]. Moreover, the cost, shelf-life and auxiliary components of the battery cells used in electric mobility, especially in Electric Vehicles (EV) or Hybrid Electric Vehicles (HEV), have drawn the attention to the sizing, downsizing and reconfiguration of the storage units composed of battery cells. Consequently, high step-up converters are required to interface the low voltage battery with the electric motor and its inverter [9]-[13].

These high voltage-gain converters are a solution to the conventional single-phase boost topologies that present some drawbacks mainly due to two reasons: 1) Extremely high losses in the power devices produced by the parasitic components and the high duty cycles needed to obtain the required output voltage. When a high duty cycle is used, an extremely high input current is demanded, therefore, high losses occur; and 2) As [5] shows, the parasitic components hamper the conventional voltage-gain at high duty cycles, i.e. when a high duty cycle is used, the voltage-gain tends to decrease because of the parasitic components [14]-[17].

Hence, several high step-up topologies have been proposed in order to deal with the problems mentioned above. For example, the switched-capacitor converter, proposed to increase the voltage-gain by adding several capacitors. However, this converter presents low efficiency due to the switching losses generated by the hard-switching operation and conduction losses in each capacitor [18]. Moreover, in order to increase the voltage-gain, several outstanding converters use techniques of built-in transformers, flyback-boost cells, voltage multipliers cells, etc. In addition, techniques of active clamping and charge pumping are used to recycle leakage energy and to absorb switching spikes [7].

Nevertheless, the high step-up converter that uses these techniques have limitations of efficiency and power density because these converters are single-phase topologies, i.e. the total input current has to flow throw the inductors, the power devices have to be selected at the full rated voltage and current, and the output capacitor is bulky. What is more, these converters use additional circuitry that increases the size of the converter.

In this context, well-known techniques reported as effective to increase the power density of power converters can be applied. This brings into scene the interleaving phases technique, which is effective because the input current can be divided into the number of phases. This way, it produces a reduction on the inductance of the input smoothing inductors, as well as a size miniaturization of the capacitive components because of the high frequency operation. Additionally, magnetic coupling represents an appealing technique in interleaved converters because a size reduction of the magnetic components can be achieved through the integration of several windings into only one core. This technique may reduce the input current ripple of the converter as well [19]-[22].

Therefore, this study addresses the problem of low power density by analyzing a novel high step-up DC-DC converter that uses the techniques of interleaving phases and magnetic coupling in order to obtain a higher voltage-gain and high power density performance. In [3] and [5], previous analyses of this outstanding topology are presented. Specifically, the magnetic core configuration and the parasitic resistance effect are employed. Nevertheless, the comparison with other outstanding high step-up has not been done. In this study, the effectiveness of the proposed converter is evaluated from the analytical point of view and by means of comparisons with outstanding interleaved topologies that offer high voltage-gain.

This chapter is organized as follows: First, the configuration and operating principle of the novel high step-up interleaved boost converter with a particular integrated coupled-inductor is presented. Second, the voltage-gain of the proposed converter is derived from the steady-state analysis. Third, each coupled-inductor configuration is introduced. The magnetic modeling of each coupled-inductor configuration is presented and later, a quantitative comparison with some recent and outstanding high step-up interleaved converters with similar configuration to the proposed converter is presented. Fourth, a parasitic analysis of the proposed converter and a comparison with outstanding converters is developed. Fifth, the modeling of the magnetic flux in each leg of the coupled-inductor is conducted as the base for the inductor designing. Finally, experimental tests of 100W prototypes are shown as a validation of the effectiveness of the proposed topology in terms of voltage-gain versus number of components.

5.2 High Step-Up Converter

The proposed high step-up converter (Figure 5.1) is a two-phase interleaved boost converter composed of a particular magnetic coupled-inductor that consists of three windings that can be installed in different core configurations. There are two windings, L_1

and L_2, connected to the power source and a third winding L_c, known as central winding, located between the cathodes of D_1 and D_2. For convenience, we define the positive terminal of L_c as the node where the cathode of D_1 and the anode of D_3 are connected.

This converter has also two power switches S_1 and S_2 which are alternatively commuted with a 180-degree phase difference between them, four diodes D_1-D_4 and one output capacitor C_o.

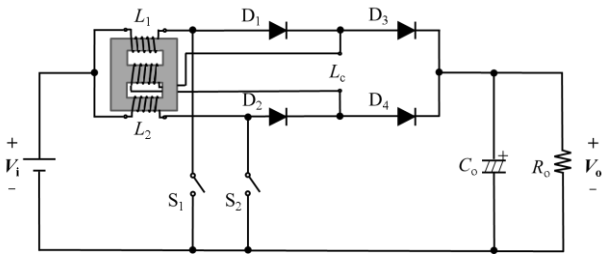


Figure 5.1. High step-up converter with coupled inductor.

Figure 5.2 shows the coupled inductor with three windings installed into only one core. The number of turns of this specific inductor may vary, which will make the voltage gain vary as well.

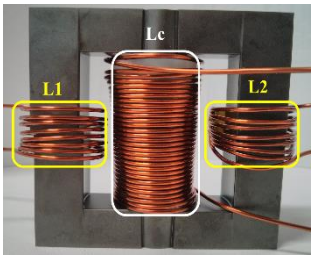


Figure 5.2. Coupled-inductor with 3 windings for a HSU converter.

At combining the high step-down converter presented in chapter 4 with the high step-up converter of this chapter, it is possible to obtain a bidirectional high step-up converter as shown in Figure 5.3. This topology can be useful for EV applications in which a bidirectional performance is required to feed the motor when the vehicle is driven and to charge the storage unit when the vehicle is braked.

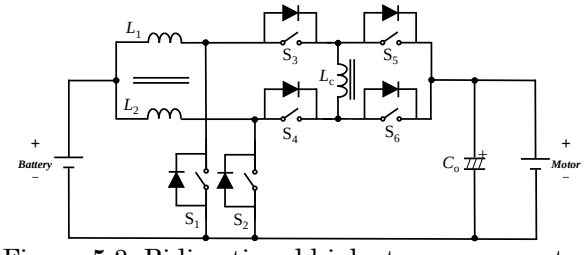
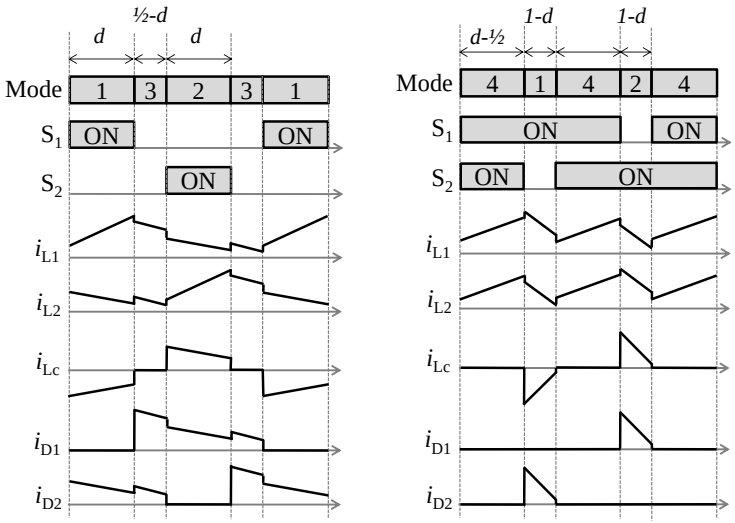


Figure 5.3. Bidirectional high step-up converter.

5.2.1 Steady state analysis

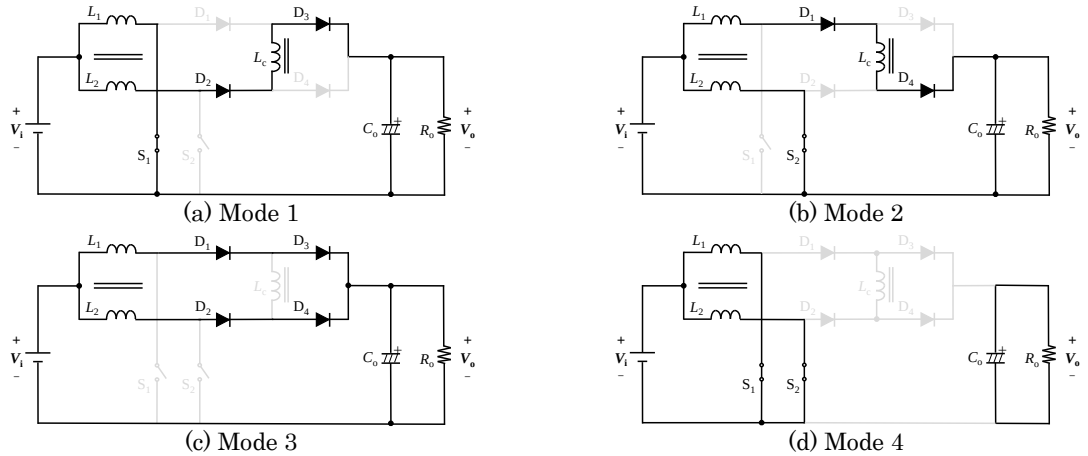
The two-phase interleaved high step-up converter presents four different operating modes corresponding to all the combinations of the ON and OFF-state of the switches, as shown in Figure 5.4. In addition, Figure 5.4 shows the operating waveforms of the proposed converter when it is under an ideal operation when the duty cycle d is lower and higher than 50%.

In this context, Figure 5.5 shows the overall operating modes of the high step-up converter.



(a) D<50% (b) D>50%

Figure 5.4. Operating waveforms.



(a) Mode 1 (b) Mode 2

(c) Mode 3 (d) Mode 4

Figure 5.5. Operating modes.

Mode 1: As Figure 5.4 and Figure 5.5(a) show, S_1 is turned ON and S_2 is turned OFF, where i_1 flows only through the external winding L_1. On the other hand, i_2 flows through L_2, D_2, D_3, L_C and C_o. Moreover, a negative voltage is induced in the central winding as a result of the voltage applied to the external windings.

Consequently, based on the two loops of Figure 5.5(a) it is possible to derive:

$$V_i = N_o \frac{\Delta\phi_1}{T_1} \tag{5.1}$$

$$V_i = N_o \frac{\Delta\phi_2}{T_1} - N_c \frac{\Delta\phi_c}{T_1} + V_o \tag{5.2}$$

where $\Delta\phi_1$, $\Delta\phi_2$ and $\Delta\phi_c$ are the magnetic flux variations in the windings L_1, L_2 and L_c, respectively. And, T_1 is the time duration of Mode 1.

Mode 2: Based on Figure 5.4 and Figure 5.5(b), S_1 is turned OFF and S_2 is turned ON, i_1 flows through L_1, D_1, D_4, L_c and C_o. In contrast, i_2 flows only through the winding L_2. In addition, a positive voltage is induced in the central winding L_c and therefore the current flows through L_c rather than through D_2 and D_3.

Taking into account the operating principle of each loop in Mode 2, it is possible to derive:

$$V_i = N_o \frac{\Delta\phi_1}{T_2} + N_c \frac{\Delta\phi_c}{T_2} + V_o \tag{5.3}$$

$$V_i = N_o \frac{\Delta\phi_2}{T_2} \tag{5.4}$$

where T_2 is defined as the time of Mode 2.

Mode 3: As Figure 5.4 and Figure 5.5(c) show, S_1 and S_2 are turned OFF and i_1 flows through L_1, D_1, D_3 and C_o; while i_2 flows through L_2, D_2, D_4 and C_o.

Based on Figure 5.5(c) and the operation explained before, we can derive:

$$V_i = N_o \frac{\Delta\phi_1}{T_3} + V_o \tag{5.5}$$

$$V_i = N_o \frac{\Delta\phi_2}{T_3} + V_o \tag{5.6}$$

where T_3 is the time duration of Mode 3.

Mode 4: Finally, as Figure 5.4 and Figure 5.5(d) show, S_1 and S_2 are turned ON, where i_1 flows only through L_1, and i_2 through L_2. All four diodes remain OFF and there is no current flowing through the central winding of the coupled inductor. Consequently, the loops expressions can be derived as:

$$V_i = N_o \frac{\Delta\phi_1}{T_4} \tag{5.7}$$

$$V_i = N_o \frac{\Delta\phi_2}{T_4} \tag{5.8}$$

where T_4 is the duration of Mode 4.

5.2.2 Central winding operation

As it was mentioned above, the magnetic component of this converter has three windings sharing the same core. In this case, there are three different magnetic fluxes circulating through the entire core, see Figure 5.6. In this coupled-inductor, the external windings are directly coupled where an air-gap is made in each external leg with the purpose of suppressing the DC flux induction.

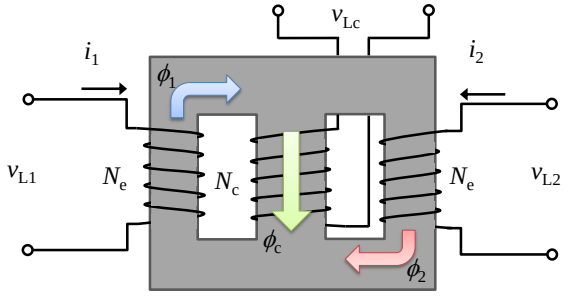


Figure 5.6. Magnetic flux in the coupled-inductor.

Taking into account the fact that the induced voltage in the central winding, produced by the applied voltage to the external windings, is presented in Modes 1 and 2, see Figure 5.4, it is possible to derive:

$$\begin{cases} v_{L1} = N_e \dfrac{d\phi_1}{dt} \\ v_{L2} = N_e \dfrac{d\phi_2}{dt} \\ v_{LC} = N_C \dfrac{d\phi_C}{dt} \end{cases} \tag{5.9}$$

where, v_{L1}, v_{L2} and v_{LC} are the external and central winding voltages, ϕ_1, ϕ_2 and ϕ_c are the external and central magnetic fluxes, and N_e and N_c are the number of turns of the external windings and the central winding respectively. Additionally, taking into account the orientation of the magnetic fluxes of Figure 5.6, it is possible to infer that:

$$\phi_C = \phi_1 - \phi_2 \tag{5.10}$$

Consequently, from (5.9) and (5.10) it is possible to obtain:

$$v_{LC} = \frac{N_c(v_{L1} - v_{L2})}{N_e} \tag{5.11}$$

Now, it is possible to define the relationship between the external windings and the central winding as the ratio N:

$$N = \frac{N_c}{N_e} \tag{5.12}$$

Finally, from (5.11) and (5.12):

$$v_{LC} = N(v_{L1} - v_{L2}) \tag{5.13}$$

In this way, the relationship between the voltage of the central winding and the voltage of the external windings is defined.

5.2.3 Voltage-gain derivation

In order to derivate the voltage gain expression of the high step-up converter, the steady-state analysis is required, therefore the following presents a review of the winding voltages of each operating mode.

Mode 1:

$$v_{L1} = v_i \tag{5.14}$$

$$v_{L2} = \frac{v_i(1+N) - v_O}{1+N} \tag{5.15}$$

Mode 2:

$$v_{L1} = \frac{v_i(1+N) - v_O}{1+N} \tag{5.16}$$

$$v_{L2} = v_i \tag{5.17}$$

Mode 3:

$$v_{L1} = v_i - v_O \tag{5.18}$$

$$v_{L2} = v_i - v_O \tag{5.19}$$

Mode 4:

$$v_{L1} = v_i \tag{5.20}$$

$$v_{L2} = v_i \tag{5.21}$$

Therefore, this converter has two sequences of voltage-gain presented at different values of duty cycle *D*. Hence, from (5.14), (5.16) and (5.18), the voltage conversion ratio, that is the ratio between the output voltage v_o and the input voltage v_i, when the duty cycle is lower than 50% is derived as:

$$M_{\mathrm{D<0.5}} = \frac{V_{\mathrm{o}}}{V_{\mathrm{i}}} = \frac{1+N}{(1+N)-D(1+2N)} \tag{5.22}$$

On the other hand, from (5.14), (5.16) and (5.20), the voltage-gain for the case when the duty cycle is higher than 50% is derived as follows:

$$M_{\mathrm{D>0.5}} = \frac{V_{\mathrm{o}}}{V_{\mathrm{i}}} = \frac{1+N}{1-D} \tag{5.23}$$

Thus, taking into account equations (5.22) and (5.23), and the values of *N*=2, 4 and 8, it was possible to construct the ideal conversion ratio according to the duty cycle as shown in Fig. 8. This figure shows the performance comparison of the proposed converter, and the conventional single-phase boost converter and the interleaved two-phase boost converter which voltage-gain is defined as follows [15]:

$$M_{\mathrm{boost}} = \frac{V_{\mathrm{o}}}{V_{\mathrm{i}}} = \frac{1}{1-D} \tag{5.24}$$

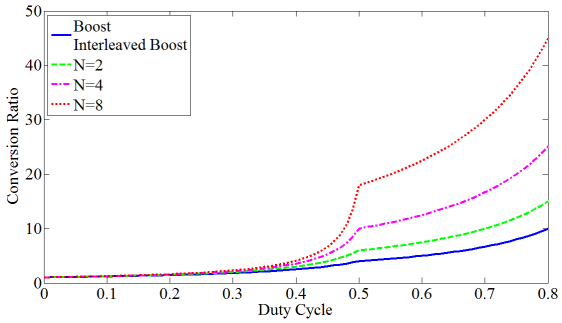


Figure 5.7. Voltage-gain of the proposed converter vs. conventional boost converters.

From this analysis, it is possible to conclude that the influence of the coupled-inductor, specifically the central winding and the arrangement of the four diodes D_1-D_4, generates a higher voltage-gain in comparison with the conventional step-up topologies.

5.2.4 Experimental validation of the HSU comparison

In order to validate and to have a complete understanding of the effectiveness of the proposed high step-up converter, a 100W prototype was constructed and experimentally tested. Therefore, five different circuits were tested. Therefore, four circuits were constructed using SiC Diodes, CoolMos, Multilayer Capacitors and four coupled-inductors with different turns ratios: N=*1*, *2*, *4* and *8*. Additionally, the two-phase interleaved boost converter with Integrated Winding Coupled-Inductor IWCI was tested as well.

These five circuits were tested at 100V of output voltage and an input voltage between a range of 3.5V and 76V, in order to evaluate different conversion ratios and different duty cycle values. Moreover, the experimental tests were set at 100 W of output power and 100 kHz of switching frequency. Table 5.1 shows a summary of the experimental parameters. Table 5.2 shows the parameters of the coupled inductors.

Table 5.1 Experimental Parameters for the Number of Turns Comparison

Parameter		Value
Input Voltage	V_i	3.5V – 76V
Output Voltage	V_o	100V
Output Power	P_o	100W
Duty Cycle	d	10%-70%
Frequency	f	100kHz

Table 5.2 Inductor Parameters for the Number of Turns Comparison.

		HSU N=1	HSU N=2	HSU N=4	HSU N=8	*IWCI* converter
Number of turns	N	External: 32 turns Center: 32 turns	External: 16 turns Center: 32 turns	External: 8 turns Center: 32 turns	External: 4 turns Center: 32 turns	External: 16 turns Center: 16 turns
Inductance	L	L_1: 1.53 mH L_2: 1.54 mH L_c: 1.87 mH	L_1: 380 µH L_2: 378 µH L_c: 1.87 mH	L_1: 98.5 µH L_2: 99 µH L_c: 1.87 mH	L_1: 25.3 µH L_2: 25.2 µH L_c: 1.87 mH	L_1: 257 µH L_2: 517 µH L_2: 525 µH
ESR	R	R_1: 820 mΩ R_2: 835 mΩ R_c: 806 mΩ	R_1: 403 mΩ R_2: 409 mΩ R_c: 806 mΩ	R_1: 50 mΩ R_2: 53 mΩ R_c: 806 mΩ	R_1: 29.2 mΩ R_2: 29.1 mΩ R_c: 806 mΩ	R_1: 3.64 Ω R_2: 3.77 Ω R_c: 670 mΩ
Air gap	L_g	0.5 mm (external legs)	0.5 mm (external legs)	0.5 mm (external legs)	0.5 mm (external legs)	2.55 mm (center leg)
Window area	A_w	642 mm²				
Sectional area	A_{core}	280 mm²				

Consequently, Figure 5.8 shows the experimental results of the selected five circuits. In this figure it is possible to validate the effectiveness of the proposed high step-up two-phase interleaved boost converter with the particular coupled-inductor. It is evident the difference between the voltage-gain of the conventional interleaved converter with the IWCI coupled-inductor and the proposed converter high step-up boost converter.

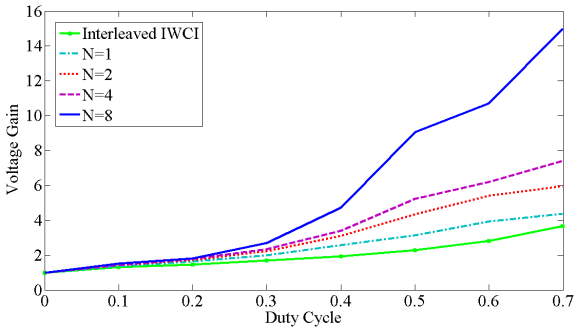


Figure 5.8. Experimental Results.

As Figure 5.8 shows, the proposed converter is more effective at duty cycles higher than 50%. In comparison with the IWCI converter, the proposed converter with a turns ratio *N=2* achieves an increment of 20% in the voltage-gain when it is operating at a duty cycle of 70%. In addition, when the converter has a turns ratio *N=8* achieves an increment of four times in the voltage-gain when it is operating at a duty cycle of 70%. However, the experimental results show lower values in comparison to the ideal cases presented by the theoretical calculation, as it is shown in Figure 5.7. This behavior is caused by the parasitic resistances and inductances presented in the coupled-inductor.

Nevertheless, even with the reduction generated by these parasitic components, the results revealed the effectiveness of the proposed converter in comparison to the ideal conventional topologies.

5.3 Analysis of Coupled Inductor Configuration

The HSU converter can be constructed with two different core configurations: The first one is the two-core coupled inductor version, which is composed of an additional winding L_C wound on normal inductors for L_1 and L_2. The second one is the integrated coupled-inductor version, which magnetically integrates the two-core coupled inductor into only one core.

In this subsection, the performance evaluation of the two coupled-inductor configurations of the proposed converter is presented. This evaluation is conducted with the purpose of establishing the suitable core configuration which offers the highest voltage-gain.

5.3.1 Coupled-inductor configurations

Two configurations of coupled inductor that achieve these features are proposed: The first one is the Integrated Coupled-Inductor (ICI), where the three windings are installed into only one EE core, in which, L_1 and L_2 are wound in the external legs of the EE core and L_c is wound in the central leg, as shown in Figure 5.2. Moreover, the external windings are directly coupled and an air-gap is installed in each external leg in order to suppress excessive DC flux induction.

On the other hand, the second configuration is the Two Cores Coupled-Inductor (TCCI), where two EE cores are used in order to integrate the windings. As Figure 5.9 shows, L_1 and L_2 are independently wound in the central leg of each EE core. Each of these windings is wound in different direction with the purpose of emulating the direct coupling of the ICI configuration. In addition, L_c is wound around the windings L_1, L_2 and the central legs of both EE cores, see Figure 5.9. The purpose of this approach is to obtain a magnetic coupling between the windings L_1, L_2 and L_c.

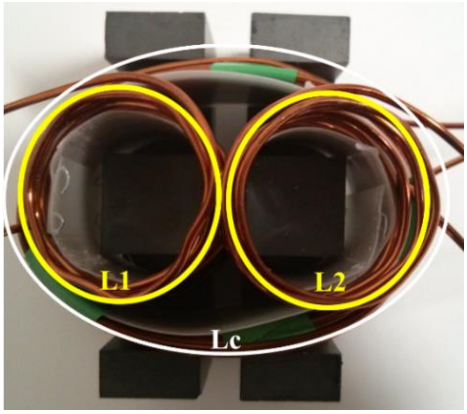


Figure 5.9. Two cores coupled-inductor.

In both configurations, there are two independent magnetic fluxes ϕ_1 and ϕ_2, and one shared flux ϕ_c as shown in Figure 5.10 and Figure 5.11.

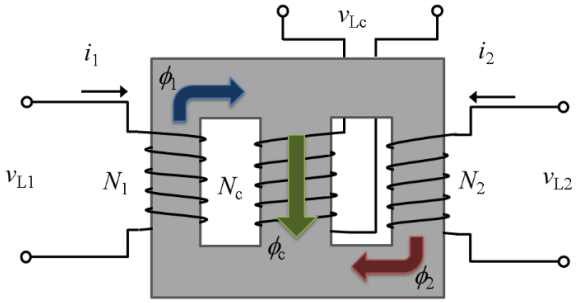


Figure 5.10. Magnetic flux in the integrated coupled-inductor.

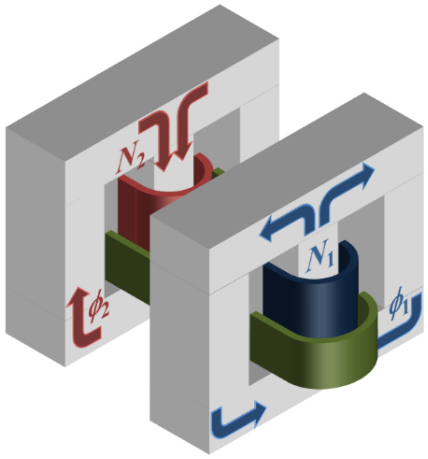


Figure 5.11. Magnetic flux in the two cores coupled-inductor.

5.3.2 Magnetic modeling

With the purpose of analyzing the current behavior of each winding in both coupled-inductor configurations ICI and TCCI, the magnetic modeling of each configuration is required.

In this case, for convenience in the calculation, a general magnetic circuit model generic for both configurations is introduced in Figure 5.12.

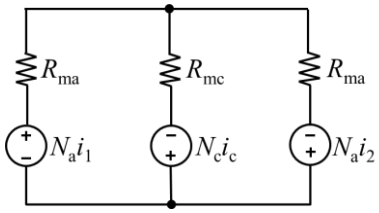


Figure 5.12. General magnetic circuit model.

In this generic model, each magneto-motive force (Ni) is applicable for both models because windings L_1 and L_2 are directly coupled while the central winding L_c is crossed by both fluxes (ϕ_1-ϕ_2).

On the other hand, the magnetic reluctances of this generic model are different in both inductor configurations. Therefore, the magnetic reluctances of the ICI configuration are defined as:

$$\begin{cases} R_{ma} = R_e \\ R_{mc} = R_c \end{cases} \tag{5.25}$$

where R_e and R_c are defined as the reluctances of the externals and central leg, respectively, of the EE core of the ICI configuration, see Figure 5.10.

While the magnetic reluctances of the TCCI configuration can be defined as:

$$\begin{cases} R_{ma} = R_c + \dfrac{R_e}{2} \\ R_{mc} = 0 \end{cases} \tag{5.26}$$

In this case, for convenience in the calculation, the reluctances of the TCCI configuration are defined according to the independent core used for the ICI.

This section introduces the deriving process of the equations (5.25) and (5.26). These equations can be derived on the basis of the magnetic modeling of each inductor configuration. In fact, this modeling procedure was conducted with the purpose of representing both configurations with only one model.

Figure 5.13 shows the magnetic model of the ICI configuration.

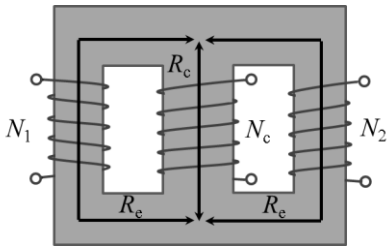


Figure 5.13. ICI magnetic circuit model.

From this model, it is possible to infer that each variable described in Figure 5.12 corresponds to the same of Figure 5.13, as follows:

$$\boldsymbol{R}_{ma} = \boldsymbol{R}_e \tag{5.27}$$

$$\boldsymbol{R}_{mc} = \boldsymbol{R}_c \tag{5.28}$$

On the other hand, the modeling of the TCCI is more complicated. Figure 5.14 shows the reluctances in each core.

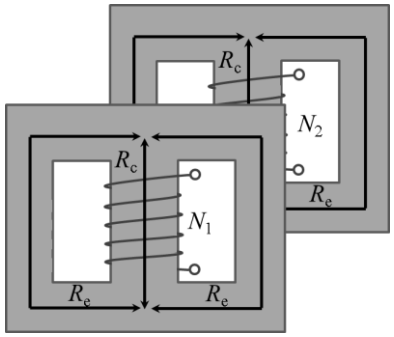


Figure 5.14. TCCI magnetic circuit model.

In addition, Figure 5.15 shows the equivalent magnetic circuits of each independent core.

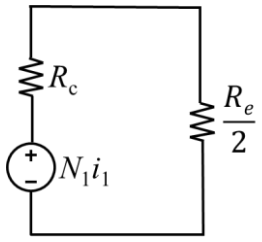


Figure 5.15. Equivalent circuit of each independent core in the TCCI configuration.

As Figure 5.15 shows, the equivalent circuit of each independent core of the TCCI configuration is simplified by the parallel of both reluctances of the external legs ($R_e/2$) plus the reluctance of the central leg R_c.

Therefore, the magnetic circuit of each independent core of the TCCI can be described as:

$$N_1 i_1 + N_c i_c = \left(R_c + \frac{R_e}{2} \right) \phi_1 \tag{5.29}$$

$$N_1 i_1 + N_c i_c = \left(R_c + \frac{R_e}{2} \right) \phi_1 \tag{5.30}$$

On the other hand, for the derivation of the reluctance of the center of both cores, where there are both central legs and air, it is necessary to consider the base of Faraday's law and Ampere's law. Therefore, in order to satisfy Eq. (5.29) and (5.30), it is possible to infer that the value of R_{mc}, in the generic model for the case of the TCCI, has to be zero.

Finally, as a conclusion, the reluctances of the TCCI can be defined as:

$$R_{ma} = R_c + \frac{R_e}{2} \tag{5.31}$$

$$R_{mc} = 0 \tag{5.32}$$

In this context, the generic model of Figure 5.12 can be applied for the windings current calculation for both inductor configuration, having in mind that the magnetic reluctances are different as it was explained before. Consequently, on the base of the Faraday's law, the magnetic loops of Figure 5.12 can be described as:

$$N_a i_1 + N_c i_c = R_{ma} \phi_1 + R_{mc} \left(\phi_1 - \phi_2 \right) \tag{5.33}$$

$$N_a i_2 - N_c i_c = R_{ma} \phi_2 - R_{mc} \left(\phi_1 - \phi_2 \right) \tag{5.34}$$

Consequently, based on the steady-state analysis and Figure 5.5(a), the central winding current during Mode 1 is defined as:

$$\boldsymbol{I}_c = -\boldsymbol{I}_2 \tag{5.35}$$

Therefore, in Mode 1, substituting (5.35) into (5.33) and (5.34) yields:

$$I_1 = \frac{\left[N_a\left(R_{ma}+R_{mc}\right)+N_cR_{ma}\right]\phi_1+\left(N_cR_{ma}-N_aR_{mc}\right)\phi_2}{N_a\left(N_a+N_c\right)} \tag{5.36}$$

$$I_2 = \frac{\left(R_{ma}+R_{mc}\right)\phi_2-R_{mc}\phi_1}{N_a+N_c} \tag{5.37}$$

Based on Figure 5.5(b), the central winding current in Mode 2 is defined as:

$$I_c = I_1 \tag{5.38}$$

Consequently, from (5.38), (5.33) and (5.34) the current of L_1 and L_2 in Mode 2 is:

$$I_1 = \frac{\left(R_{ma}+R_{mc}\right)\phi_1-R_{mc}\phi_2}{N_a+N_c} \tag{5.39}$$

$$I_2 = \frac{\left[N_a\left(R_{ma}+R_{mc}\right)+N_cR_{ma}\right]\phi_2+\left(N_cR_{ma}-N_aR_{mc}\right)\phi_1}{N_a\left(N_a+N_c\right)} \tag{5.40}$$

Then, taking into account the steady state analysis and Figure 5.5(c), there is no current flowing through the central winding during Mode 3. Thereby, it is possible to derive:

$$I_1 = \frac{1}{N_a}\left[\left(R_{ma}+R_{mc}\right)\phi_1-R_{mc}\phi_2\right] \tag{5.41}$$

$$I_2 = \frac{1}{N_a}\left[\left(R_{ma}+R_{mc}\right)\phi_2-R_{mc}\phi_1\right] \tag{5.42}$$

Finally, as Figure 5.5(d) shows, there is no presence of current flowing through the central winding during Mode 4 and therefore the current of L_1 and L_2 present the same value of Eq. (5.41) and (5.42), respectively.

Conclusively, and based on the windings current presented in each mode, it is possible to see that the current flowing through each winding has a different behavior dependent on the magnetic reluctance of each configuration.

Nonetheless, the total input current, i.e. I_1+I_2, is always equal to $R_{ma}/N_a \cdot(\phi_1+\phi_2)$, regardless to the operating modes. This indicates that the waveform of the total input current is continuous because fluxes ϕ_1 and ϕ_2 should be continuous according to Faraday's law. Therefore, the proposed converter can offer small input current ripple, although the

waveform of each phase current can have significant discontinuity.

5.3.3 Experimental validation

In order to verify the operating principle of the proposed converter, and to compare the effectiveness of each inductor configuration, three 100W prototypes were constructed and experimentally tested.

The experimental tests evaluate the voltage-gain of the two types of coupled-inductor and the input current of the proposed converter. Table 5.3 shows the experimental parameters of the ICI and TCCI prototypes and Figure 5.16 shows the experimental setup of the ICI converter.

Table 5.3 Experimental Parameters for Inductor Configuration Evaluation.

		ICI	TCCI
Input Voltage	V_i	10.1V – 80.7V	12.5V – 82.4V
Output Voltage	V_o	100V	
Output Power	P_o	100W	
Frequency	f	30kHz	
Number of turns	N	External: 16 turns Center: 32 turns	External: 16 turns Center: 32 turns
Inductance	L	L_1: 380 µH L_2: 378 µH L_c: 1.87 mH	L_1: 210 µH L_2: 231 µH L_c: 1.86 mH
Window area	A_w	642 mm^2	396 mm^2
Sectional area	A_{core}	280 mm^2	247 mm^2
Volume	V_e	40420 mm^3	27100 mm^3 each

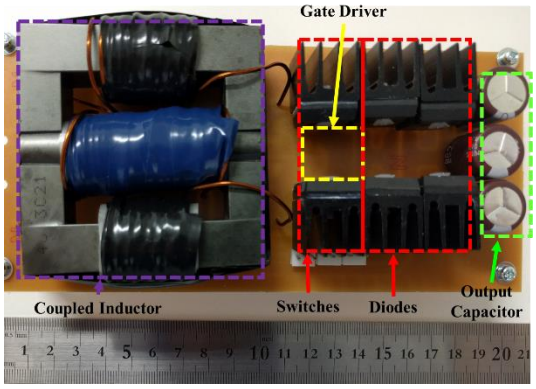


Figure 5.16. Experimental setup.

These prototypes were constructed using SiC Diodes, CoolMos, Multilayer and Electrolytic Capacitors and the mentioned coupled-inductors with a ratio of turns of $N=2$. In fact, the third prototype corresponds to the conventional interleaved two-phase boost

converter which is constructed with the purpose of comparing the voltage-gain of the proposed converter.

Figure 5.17 shows the experimental results of the voltage-gain of the proposed high step-up converter with the two configurations of coupled-inductors. This figure also shows the theoretical voltage-gain at *N=2*. In addition, the experimental voltage-gain of the conventional two-phase interleaved boost converter is presented as well.

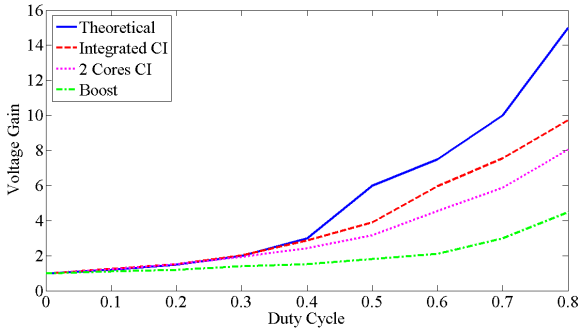


Figure 5.17. Voltage-gain vs. duty cycle.

The results revealed that both prototypes of the proposed converter show a higher voltage-gain compared to the conventional boost chopper, particularly in duty cycles higher than 0.5. In addition, the voltage-gain of the integrated coupled-inductor was 20% higher than the two cores coupled-inductor when the converter is operating at a duty cycle of 80%.

However, the experimental results present lower voltage-gain in comparison to the theoretical calculation; this may be caused by the parasitic resistance and the stray inductance in the coupled-inductor [25]. Consequently, the effectiveness of the integrated coupled inductor in the proposed converter is demonstrated.

Moreover, Figure 5.18 shows the experimental waveforms of the gate-source voltage V_{GS1} and the winding current i_{L1} of the proposed high step-up converter with the integrated coupled-inductor as a validation of the operating waveforms illustrated in Figure 5.5.

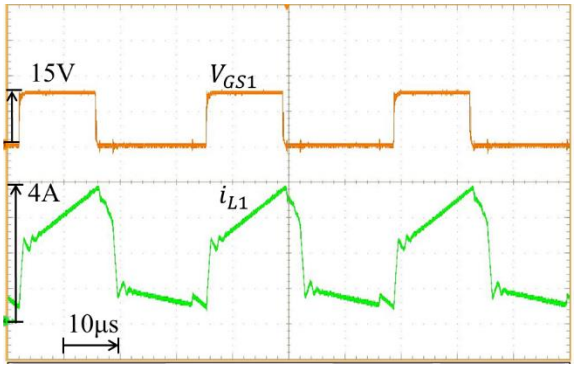


Figure 5.18. Winding current of the ICI prototype.

Based on Figure 5.18, it is possible to affirm that the winding current i_{L1} and its dual i_{L2} have a discontinuous behavior. However, the integration of these two waveforms shapes a continuous input current, as shown in Figure 5.19.

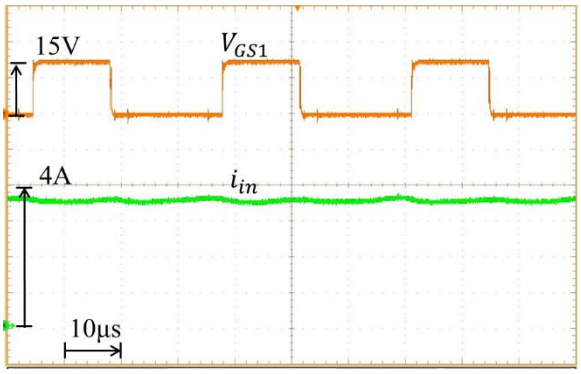


Figure 5.19. Input current of the ICI prototype.

Finally, the input current ripple i_{in} of the proposed converter with ICI configuration was measured and compared with the input current ripple of the conventional interleaved two-phase boost converter. As a result, the proposed converter presents a normalized input current ripple of 8.33%, while the conventional topology has a ripple of 10%. Therefore, the effectiveness of the proposed converter is validated.

5.4 Comparison of HSU converters

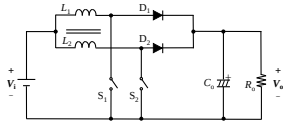
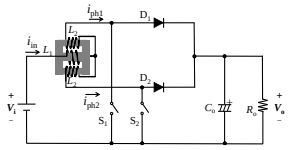
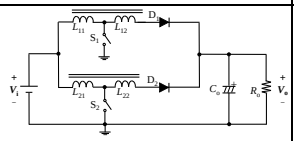
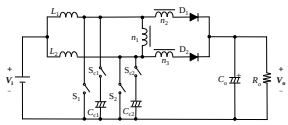
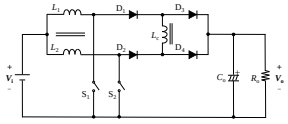
With the purpose of showing the effectiveness of the proposed converter in voltage-gain and number of additional components, a performance comparison of the proposed converter with several outstanding high step-up converters that use the techniques of interleaving converters and magnetic coupling was conducted. In this comparison, the conventional two-phase interleaved converter with conventional inductors and with the Integrated Winding Coupled-Inductor (IWCI) are compared as well. The IWCI converter was selected because the coupled inductor is composed of three windings, which is similar to the proposed converter [23].

Moreover, the high step-up converters published in [24] and [25] were selected because they are improved topologies proposed in the recent years that offer higher voltage-gains than the conventional high step-up converters. These selected converters and the proposed converter have the similarity of the voltage-gain dependency on the turns ratio N of the coupled-inductor or of the built-in transformers.

In this context, Table 5.4 shows the characteristics comparison of the mentioned high step-up converters. In this table, the number of components and the voltage-gains are evaluated. Based on the comparison of Table 5.4, it is possible to conclude that the proposed converter has fewer components in comparison to other outstanding high step-up topologies. Specifically, the proposed topology offers a reduction in the number of magnetic cores and an addition of two diodes. Therefore, the proposed converter presents

a lower mass, volume and cost regarding the magnetic components. Based on this comparison, it is possible to infer that the proposed converter presents higher power density.

Table 5.4 HSU Converters Comparison

Converter	Configuration	Conversion Ratio	Sw	D	Wind	Cores	Cap
Conventional Interleaved Boost		$M = \frac{1}{1-D}$	*2*	*2*	*2*	*1*	*1*
Interleaved Boost IWCI		$M = \frac{1}{1-D}$	*2*	*2*	*3*	*1*	*1*
Converter published in [24]		$M = \frac{1+ND}{1-D}$	*2*	*2*	*4*	*2*	*1*
Converter published in [25]		$M = \frac{1+N}{1-D}$	*2 Main 2 for snubbers*	*2*	*5*	*3*	*3*
Proposed		$M_{D<0.5} = \frac{1+N}{(1+N)-D(1+2N)}$ $M_{D>0.5} = \frac{1+N}{1-D}$	*2*	*4*	*3*	*1*	*1*

Finally, the voltage-gain of the converters compared in Table 5.4 is plotted and shown in Figure 5.20. Based on this figure, it is possible to determine that the IWCI converter presents the same conversion ratio as the conventional boost and the interleaved boost converter. Nevertheless, the voltage-gain of the converter published in [24] is much higher than the one of the conventional interleaved boost converter and several high step-up converters reported in the literature. Additionally, the converter published in [25] presents a higher conversion ratio than the converter published in [24] due to the presence of a built-in transformer and some voltage clamp circuits. Finally, the proposed converter presents the same conversion ratio than the converter published in [25] at duty cycles higher than 50%. However, it is necessary to take into account that the converter published in [25] uses four switches, two diodes and five windings disposed in three cores, while the proposed converter uses two switches, four diodes and three windings disposed in only one core. Thereby, based on the fact that magnetic components are the greatest contributors to the mass and volume in DC-DC converters, it is possible to conclude that the proposed converter exhibits better advantages than the compared high step-up converters.

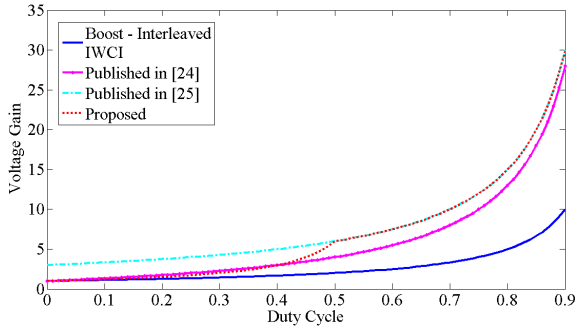


Figure 5.20. Voltage-gain comparison according to the duty cycle.

5.5 Parasitic Resistance Analysis

The analyzed converter presents a high voltage-gain performance, compared to the conventional single phase and two-phase interleaved converters. However, it is important to consider the parasitic effects, especially in the coupled-inductor in order to identify their consequences on the voltage-gain performance. Thus, the study of the equivalent parasitic resistance in series in the coupled-inductor and its effect on the converter behavior is required.

Each component of every converter presents parasitic effects which highly affect the performance of the power converter and specially the voltage-gain in DC-DC applications. Consequently, in order to have a better understanding of the capabilities of each topology presented above, it is important to analyze the effect of the parasitic components in the voltage conversion. Figure 5.21 shows the equivalent circuit of a two-phase interleaved boost converter, including the parasitic components, where R_S is the power source resistance, L is the filter inductance, R_L is the resistance of the inductor's winding (AC and DC), C_X is the equivalent parasitic capacitance of the transistor, R_{DSon} is the static drain-source on-state resistance, V_F is the forward voltage of the diode, R_D is the diode resistance, C_O is the output capacitance, R_C is the parasitic resistance of the output capacitor and R_o is the load resistance [3].

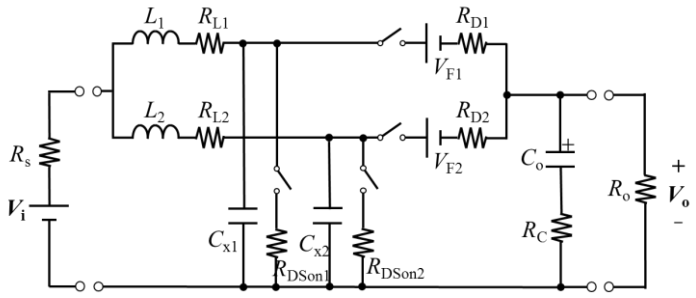


Figure 5.21. Equivalent circuit of the two-phase interleaved boost converter.

Nevertheless, in most cases, the parasitic resistances presented in the inductor's windings might produce the biggest impact to the voltage-gain [26]. Furthermore, the parasitic resistance of the free-wheeling diodes and the on-state resistance of the power

switches might be included, without loss of generality, in the value R_L. Moreover, in most cases, the parasitic resistance of the windings is much higher than the transistor's on-state resistance and the diode resistance. Therefore, the transistor's on-state resistance and the diode resistance are almost negligible for the voltage-gain analysis.

5.5.1 Parasitic resistance effect

Figure 5.22 shows the proposed high step-up interleaved boost converter with the parasitic resistances of the windings presented in the coupled-inductor. In this figure, switches S_3 - S_6 were replaced by four diodes D_1 - D_4. In addition, R_{L1}, R_{L2} and R_{Lc} are defined as the equivalent parasitic resistance in series of each external winding and the central winding, respectively. In addition, for analytical convenience, the following equations are assumed:

$$R_L = R_{L1} = R_{L2} = \frac{R_{Lc}}{N} \tag{5.43}$$

$$i_L = i_{L1} = i_{L2} \tag{5.44}$$

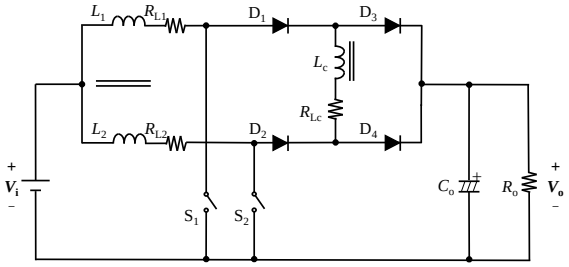
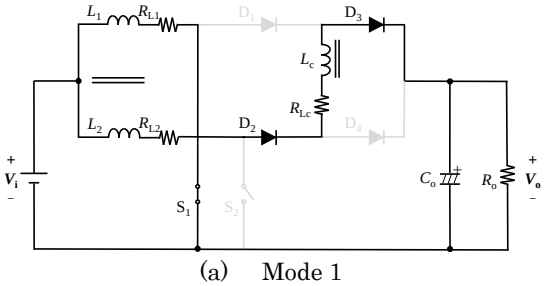
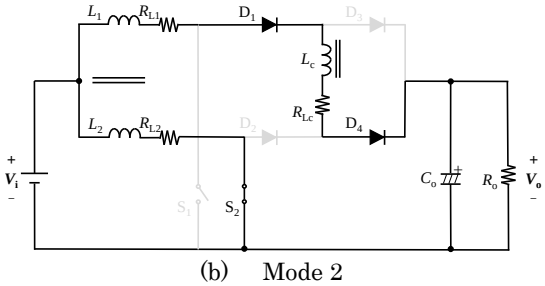


Figure 5.22. HSU converter with parasitic winding resistances.

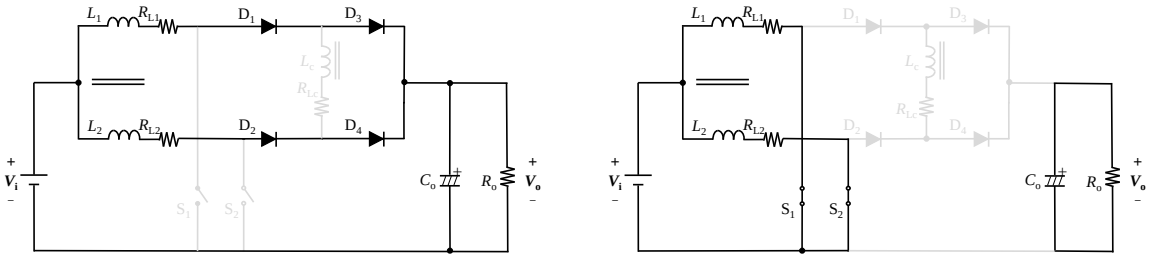
As a matter of fact, equations (5.43) and (5.44) are valid when the two phases are structurally symmetric, the windings of the external and central legs are composed of wires with the same cross-section and the magnetic core has the same sectional area.



(a) Mode 1



(b) Mode 2



(c) Mode 3 (d) Mode 4

Figure 5.23. Operating modes of the converter with parasitic resistance.

In addition, all switches in the bidirectional converter can be considered as a resistor in their on-state and the diodes in the step-up converter can be considered as a resistor based on their diode resistance. Thus, the parasitic resistance of the four diodes D_1- D_4 can be included in the value of the parasitic resistance of the central winding R_{Lc}. In addition, the parasitic resistance of the power switches S_1 and S_2 can be included in the value of resistance of each external winding R_{L1}, R_{L2}, respectively. This assumption is made on the basis that the parasitic resistance presented in the windings is much higher than the on-state and the diode resistance.

With the purpose of understanding the high step-up operation with the effect of the described parasitic resistance presented in the proposed interleaved converter, steady-state analysis is conducted. Thus, it is important to consider that the converter has four different operating modes corresponding to all the different combinations of the ON and OFF-state of the switches, as shown in Figure 5.4.

Mode 1: As shown Figure 5.23(a), S_1 is turned ON and S_2 is turned OFF, where the current of the phase 1 i_1 conducts only through the external winding L_1 and its resistance R_{L1}. On the other hand, the current of the phase 2 i_1 conducts through L_2, its resistance R_{L2}, D_2, D_3, L_c, R_{Lc} and C_o. This is possible because of a negative voltage is induced in the central winding and the corresponding drop voltage of R_{Lc}, as a result of the voltage applied to the external windings.

Mode 2: Based on Figure 5.23(b), S_1 is turned OFF and S_2 is turned ON, i_1 conducts through L_1, D_1, D_4, L_c and C_o, consequently a drop voltage appears in R_{L1}. In addition, i_2 conducts only through the external winding L_2 and its resistance R_{L2}. Due to the positive voltage induced in the central winding, therefore the current flows through L_c instead of through D_2 and D_3.

Mode 3: As Figure 5.23(c) shows, S_1 and S_2 are turned OFF and i_1 conducts through L_1, R_{L1}, D_1, D_3 and C_o. At the same time, i_2 flows through L_2, R_{L2}, D_2, D_4 and C_o. In this mode, there is no current flowing through the central winding of the coupled-inductor and therefore there is not voltage drop due to R_{Lc}.

Mode 4: With the base of Figure 5.23(d), S_1 and S_2 are turned ON, where i_1 flows only through L_1 and its resistance R_{L1}; and i_2 conducts through L_2 and R_{L2}. All four diodes do not operate and there is no current flowing through the central winding of the coupled inductor and no voltage drop in R_{Lc}.

Based on the operation of Mode 1 and the assumption of equations (5.43) and (5.44), the following equations are derived:

$$v_{L1} = V_i - i_L R_L \tag{5.45}$$

$$v_{L2} = V_i - i_L R_L + v_{Lc} - i_L R_{Lc} - V_o \tag{5.46}$$

$$i_{Co} = i_L - \frac{V_o}{R_o} \tag{5.47}$$

Thus, replacing equations (5.13) and (5.43) into (5.46), the next equation is obtained:

$$v_{L2} = \frac{(v_i - i_L R_L)(1+N) - N i_L R_L - V_o}{(1+N)} \tag{5.48}$$

In addition, in the case of Mode 2:

$$v_{L1} = V_i - i_L R_L - v_{Lc} - i_L R_{Lc} - V_o \tag{5.49}$$

$$v_{L2} = V_i - i_L R_L \tag{5.50}$$

$$i_{Co} = i_L - \frac{V_o}{R_o} \tag{5.51}$$

Therefore, replacing equations (5.13) and (5.43) into (5.49) produces:

$$v_{L1} = \frac{(V_i - i_L R_L)(1+N) - N i_L R_L - V_o}{(1+N)} \tag{5.52}$$

In addition, the analysis for the Mode 3 is shown as follows:

$$v_{L1} = v_i - i_L R_L - V_o \tag{5.53}$$

$$v_{L2} = v_i - i_L R_L - V_o \tag{5.54}$$

$$i_{Co} = 2i_L - \frac{V_o}{R_o} \tag{5.55}$$

Finally, for Mode 4:

$$v_{L1} = v_i - i_L R_L \tag{5.56}$$

$$v_{L2} = v_i - i_L R_L \tag{5.57}$$

$$i_{Co} = -\frac{V_o}{R_o} \tag{5.58}$$

D<50%: Based on Figure 5.4(a) and Figure 5.23, the case of duty cycles lower than 50% presents the operating modes 1, 2 and 3. Therefore, from (5.45), (5.49), (5.53), the output current analysis, and the relationship between every mode and the duty cycle, the voltage-gain with the parasitic effect is given by:

$$M_{D<0.5} = \frac{1+N}{\left[(1+N)-D(1+2N)\right]+\frac{R_L}{R_o}\left(\frac{(1+ND)(1+N)}{2(1-D)}\right)} \tag{5.59}$$

D>50%: On the other hand, according to Figure 5.4(b), the case of duty radio higher than 50% presents the operating modes 1, 2 and 4. Therefore, from (5.45), (5.49), (5.56), the output current analysis, and the relation between every mode and the duty cycle, the voltage-gain is given by:

$$M_{D>0.5} = \frac{1+N}{1-D+\frac{R_L}{R_o}\left(\frac{(1+N-ND)(1+N)}{2(1-D)}\right)} \tag{5.60}$$

Consequently, from (5.59) and (5.60) it is possible to establish the complete voltage conversion performance. Therefore, Figure 5.24 shows the conversion ratio according to the duty cycle for the proposed converter with a number of turns ratio of N=2.

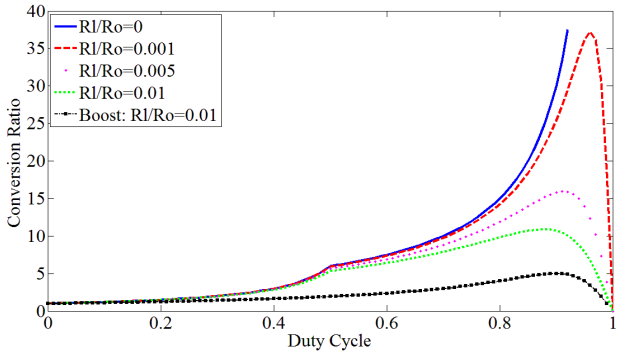


Figure 5.24. Non-Ideal conversion ratio vs. Duty cycle.

In addition, Figure 5.24 shows the comparison of a converter with different ratios of winding resistance and output resistance. Finally, the conversion ratio of the conventional boost with a resistance ratio of R_l/R_o=0.01 is evaluated having into account that its conversion ratio with parasitic resistance effect for all the duty cycle cases is defined as follows [17], [18]:

$$M_{\text{boost}} = \frac{1}{(1-D)\left(1+\frac{R_{\text{L}}}{R_{\text{o}}(1-D)^2}\right)} \tag{5.61}$$

Conclusively, the parasitic resistance in series considerably affects the voltage-gain of the proposed converter. However, in comparison with the conventional topologies, is evident the high step-up operation which presents higher voltage-gain at the same ratio of parasitic resistance and output load.

5.5.2 Experimental validation

In order to have a validation and a complete understanding of the effectiveness of the proposed high step-up converter and the effect of the parasitic resistance presented in the windings of the proposed coupled-inductor, a 100W prototype was constructed and experimentally tested.

This prototype was constructed using Silicon Carbide Diodes, CoolMos transistors, Multilayer Ceramic Capacitors and a TDK PC40 Ferrite core with 3 windings with a number of turns ratio of $N = 2$. The semiconductors and the capacitors were chosen due to its low ESR in order to reduce its effect on the voltage-gain.

Thus, this prototype was tested with the parameters shown in Table 5.5 where four different loads were installed and drive at the same output power in order to have a constant parameter of power for convenience in the comparison.

Table 5.5 Experimental Parameters for Parasitic Analysis of the HSU

Resistance Ratio	R_L/R_o	0.0035	0.0045	0.0071	0.0106
Load	R_o	200 ohms	154.8 ohms	98.8 ohms	65.8 ohms
Input Voltage	V_i	110.3V – 8.5V	97.5V – 8.04V	78.9V-7.44V	65.5V – 7.2V
Output Voltage	V_o	140V	122.94V	98.08V	79.99V
Output Power	P_o	98.98W	98.43W	98.24W	97.38W
Frequency	f_{sw}	30 kHz			
Number of Turns	N	External: 16 turns Center: 32 turns			
Inductance	L	L_1: 380 µH L_2: 378 µH L_c: 1.87 mH			
Parasitic Resistance	R	R_{L1}: 703 mΩ R_{L2}: 699 mΩ R_{Lc}: 1.41 Ω			

In addition, the experimental parameters are arranged so that the voltage drops at the diodes are ignorable because the parasitic resistance of the windings is much larger. It is important to mention that the resistance of the semiconductor is not ignorable. But, in

this experiment, for simple verification of the proposed analysis, a coupled inductor with a great parasitic resistance was used.

Consequently, Figure 5.25 shows the experimental results of the circuit with four loads in comparison with the theoretical performance of the proposed converter with $N = 2$ without parasitic resistance. Based on Figure 5.25, the effect of the parasitic resistance of the coupled-inductor windings in the voltage-gain performance is validated. However, it is evidently the difference between the conversion ratios of the conventional boost converter, shown in Figure 5.24, and the proposed converter with parasitic resistances.

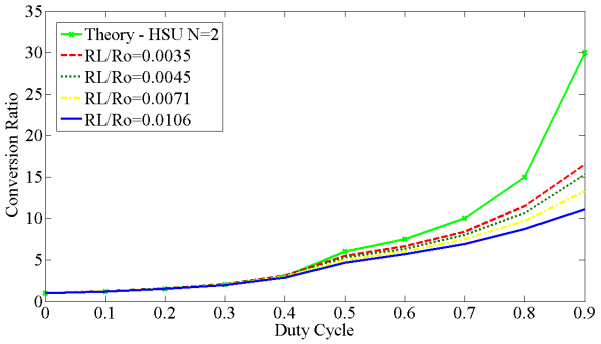


Figure 5.25. Conversion ratio tested vs. Duty cycle.

Finally, with the purpose of validating the parasitic analysis, Figure 5.26 shows the experimental results of the prototype with a ratio of $R_L/R_o = 0.0035$ and the theoretical values obtained from the equations (26) and (27). In addition, the ideal performance of the proposed converter when there is no parasitic resistance presented in the coupled-inductor is shown in Figure 5.26. Therefore, it is inferred that theoretical and experimental waveforms have a close performance.

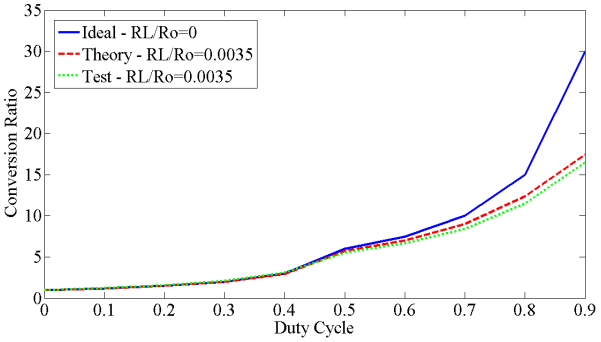


Figure 5.26. Ideal, theoretical and tested performance with RL/Ro=0.0035.

Finally, in order to have a better understanding of the advantages of the proposed high step-up converter, several efficiency tests were performed. In these tests, the ratios of R_L/R_o, studied in the previous section, were evaluated in order to get the converter efficiency under the parasitic resistance effect.

Figure 5.27 shows the efficiency experimental tests where is possible to see the influence of the parasitic resistances in the total efficiency of the converter; when the parasitic resistance increases the efficiency decreases. At the same time, when the duty

cycle is increased the efficiency is drastically affected due to the increasing of the input current.

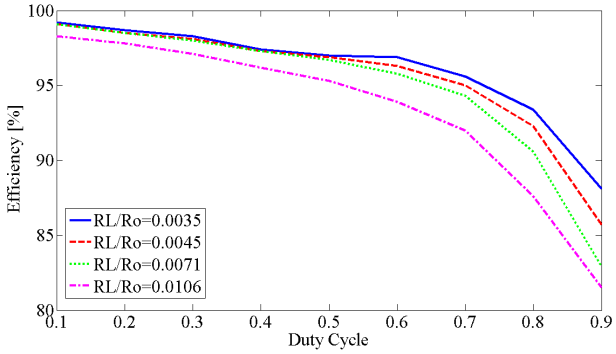


Figure 5.27. Efficiency tested vs. duty cycle.

Conclusively, in order to design a high step-up converter to be applied in EV applications, it is important to take into account the relation between the parasitic resistance of the converter and the load with the purpose of increasing the efficiency of the converter.

5.6 Parasitic Analysis Comparison

This sub-section focuses on the study and comparison of several outstanding high step-up topologies with the potential of being applied in electric mobility. Specifically, this comparison evaluates the voltage-gain of the selected converters looking for a suitable topology capable of offering a high voltage-gain with a few additional components. In addition, the effect of the parasitic components of each topology on the voltage-gain is evaluated as well.

For this comparative analysis, the influence of the inductors' parasitic resistance on the voltage-gain is evaluated. These calculations are conducted using small-ripple approximation, voltage-second balance and capacitor-charge balance.

5.6.1 Interleaved boost converter

Figure 5.28 shows the interleaved boost converter with the parasitic resistances of the coupled-inductor.

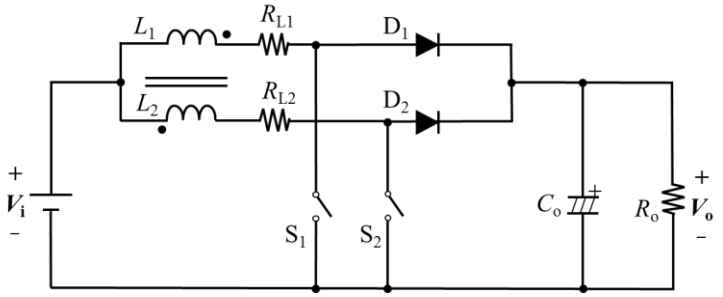


Figure 5.28. Two-phase interleaved boost converter with parasitic resistances.

In this context, for analytical convenience and assuming that the two phases are structurally symmetric and the windings are composed of wires with the same cross-sectional area, it is possible to state:

$$R_{\mathrm{L}} = R_{\mathrm{L1}} = R_{\mathrm{L2}} \tag{5.62}$$

$$i_{\mathrm{L}} = i_{\mathrm{L1}} = i_{\mathrm{L2}} \tag{5.63}$$

where $i_{L1,2}$ are the winding current in each phase. Then, the steady-state analysis is conducted where each of the four operating modes is evaluated. As a result, it is possible to obtain the voltage-gain with the parasitic effect as follows:

$$M_{\mathrm{boost}} = \frac{1}{(1-D)\left(1+\dfrac{R_{\mathrm{L}}}{R_{\mathrm{o}}(1-D)^2}\right)} \tag{5.64}$$

Figure 5.29 shows the voltage-gain of the two-phase interleaved boost converter considering several values of parasitic resistance ratio between the windings and the load (R_L/R_O). The ratio R_L/R_O is used because it is an effective way to measure the effect of the parasitic resistance in general conditions, i.e. specific parameters are not required for the evaluation.

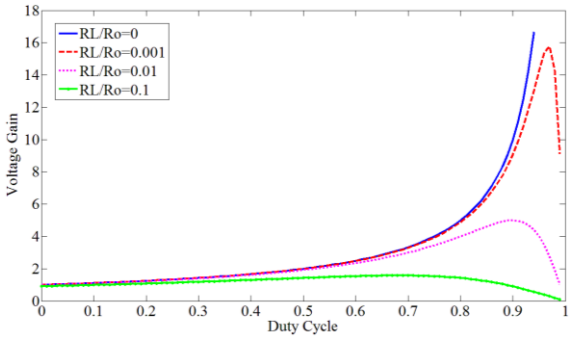


Figure 5.29. Non-ideal voltage-gain of the interleaved boost converter.

5.6.2 Interleaved tapped-inductor converter

In the case of the interleaved tapped-inductor converter, the parasitic analysis is conducted taking into account the same assumptions of the basic interleaved boost converter. As Figure 5.30 shows, the tapped-inductor presents four parasitic resistances, where it is possible to define:

$$R_{\mathrm{L1}} = R_{\mathrm{L11}} = R_{\mathrm{L21}} \tag{5.65}$$

$$R_{\mathrm{L2}} = R_{\mathrm{L21}} = R_{\mathrm{L22}} \tag{5.66}$$

$$R_{L2} = NR_{L1} \tag{5.67}$$

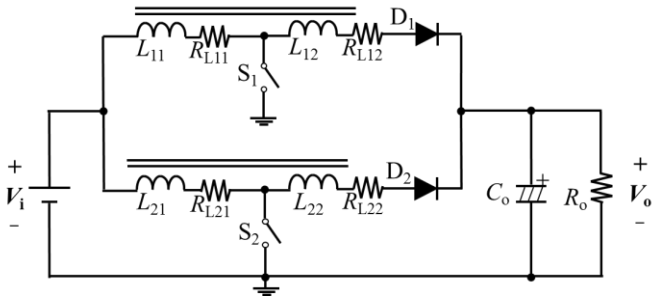


Figure 5.30. Interleaved tapped-inductor converter with parasitic resistances.

Consequently, based on the steady state analysis presented in [26], it is possible to derive:

$$M_T = \frac{(1+ND)(1-D)}{\frac{R_{L1}}{R_o}D(1+N)^2 + \frac{R_{L1}+R_{L2}}{R_o}(1-D) + (1-D)^2} \tag{5.68}$$

Figure 5.31 shows the voltage-gain of the two-phase interleaved tapped-inductor converter when it has a tapped-inductor of $N=2$. It means that R_{L2} is twice R_{L1} if the windings are structurally symmetric and use the same wire. In addition, Figure 5.31 presents several voltage-gains corresponding to some parasitic resistance ratios between the primary windings and the load (R_{L1}/Ro).

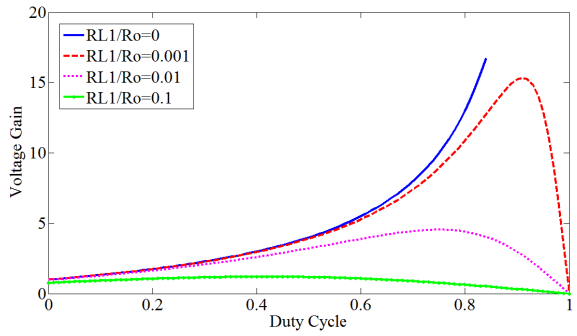


Figure 5.31. Non-ideal voltage-gain of the tapped-inductor converter.

5.6.3 Super tapped-inductor converter

Figure 5.32 shows the defined super single-phase tapped-inductor converter with parasitic resistances. Similarly to the tapped inductor converter, this topology presents two parasitic resistances R_{L1} and R_{L2}.

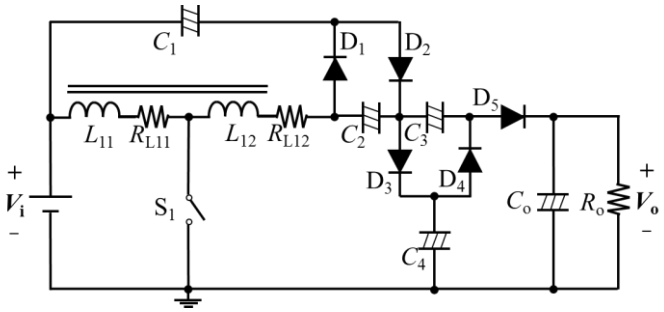


Figure 5.32. Super tapped-inductor converter with parasitic resistances.

Taking into account the voltage-gain derivation presented in [27], it is possible to obtain the voltage-gain according to the duty cycle and the parasitic resistance ratio R_{L1}/Ro.

$$M_S = \frac{\dfrac{N(2+D)+3}{1-D}}{1+\dfrac{R_{L1}}{R_o}\left(\dfrac{3(N+1)A}{(1-D)^2}\right)+\dfrac{2R_{L1}B+R_{L2}(4+5D)}{D(1-D)R_o}} \tag{5.69}$$

where

$$A = N(2+D)+3 \tag{5.70}$$

$$B = 2N\left[N(2+D)+3\right] \tag{5.71}$$

From (5.69), Figure 5.33 and Figure 5.34 are plotted showing the voltage-gain of the defined super tapped-inductor converter when it has a tapped-inductor with $N=2$. Figure 5.33 presents the voltage-gain for the parasitic resistance ratios evaluated in the previous subsections (0, 0.001, 0.01 and 0.1). Nevertheless, at these values, the effect of the parasitic resistance is quite high. Consequently, in order to see a smooth parasitic impact on the voltage-gain of this converter, Figure 5.34 shows the voltage-gain for much smaller ratios (0.0005, 0.0001 and 0.001).

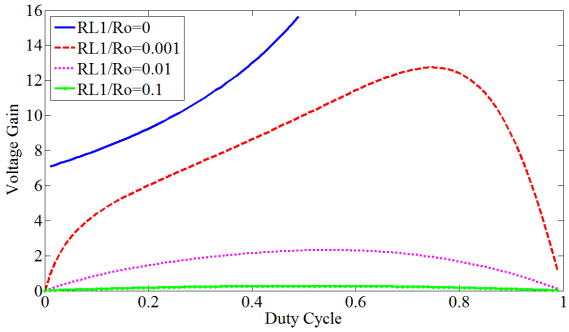


Figure 5.33. Non-ideal voltage-gain of the super tapped-inductor converter for R_{L1}/R_o=0.1-0.001.

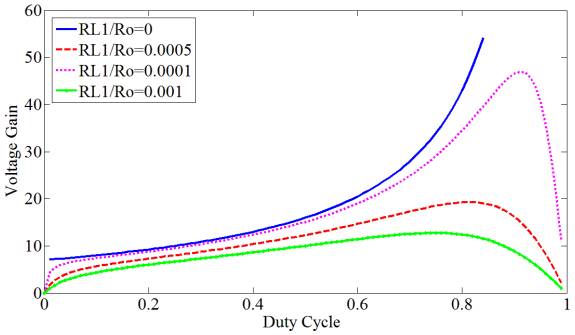


Figure 5.34. Non-ideal voltage-gain of the super tapped-inductor converter for R_{L1}/R_o=0.001-0.0005.

5.6.4 Voltage-gain comparison

With the purpose of comparing the effectiveness of each selected converter, a voltage-gain comparison was made taking into account the operating principle of each converter described above: The interleaved boost converter, the interleaved tapped-inductor converter, the super tapped-inductor converter, and the IWCI high step-up converter.

Firstly, it is evident the advantage of the magnetic coupling technique because each of the selected topologies uses coupled-inductors, tapped-inductors and integrated coupled-inductors, where the common factor is the magnetic integration into only one magnetic core. Consequently, with the exception of the conventional boost converter, all selected converters have the similarity of the voltage-gain dependence on the turns ratio N of the coupled-inductor or tapped-inductors.

In summary, Table 5.6 shows the characteristic comparison of the mentioned high step-up converters. In this table, the ideal voltage-gain, the non-ideal voltage-gain (considering the parasitic resistances), and the number of components (switches, diodes, inductors and capacitors) are compared.

Based on the ideal voltage-gain of Table 5.6, it is possible to conclude that the converters that offer a few additional components in comparison to the conventional interleaved boost converters are the tapped-inductor and the IWCI high step- up converter. Therefore, these converters might present lower mass, volume and cost in terms of semiconductor devices, magnetic and capacitive components. On the other hand, it is possible to compare the voltage-gain behavior of each converter as well. This comparison, presented in Figure 5.35, is carried out using a fair evaluation of the same turns ratio $N=2$.

Table 5.6 HSU Converters Comparison (Including Parasitic Resistances).

Converter	Ideal Voltage-gain *M*	Voltage-gain with Parasitic Effects *M*	Number of Components			
			Sw	Di	Win	C
Interleaved Boost	$\frac{1}{1-D}$	$\frac{1}{(1-D)\left(1+\frac{R_L}{R_o(1-D)^2}\right)}$	2	2	2	1
Tapped-Inductor	$\frac{1+ND}{1-D}$	$\frac{(1+ND)(1-D)}{\frac{R_{L1}}{R_o}D(1+N)^2+\frac{R_{L1}+R_{L2}}{R_o}(1-D)+(1-D)^2}$	2	2	4	1
Super Tapped-Inductor	$\frac{N(2+D)+3}{1-D}$	$\frac{\frac{N(2+D)+3}{1-D}}{1+\frac{R_{L1}}{R_o}\left(\frac{3(N+1)A}{(1-D)^2}\right)+\frac{2R_{L1}B+R_{L2}(4+5D)}{D(1-D)R_o}}$	1	5	2	5
IWCI	$_{D<0.5}=\frac{1+N}{(1+N)-D(1+2N)}$ $_{D>0.5}=\frac{1+N}{1-D}$	$_{D<0.5}=\frac{1+N}{[(1+N)-D(1+2N)]+\frac{R_L}{R_o}\left(\frac{(1+ND)(1+N)}{2(1-D)}\right)}$ $_{D>0.5}=\frac{1+N}{1-D+\frac{R_L}{R_o}\left(\frac{(1+N-ND)(1+N)}{2(1-D)}\right)}$	2	4	3	1

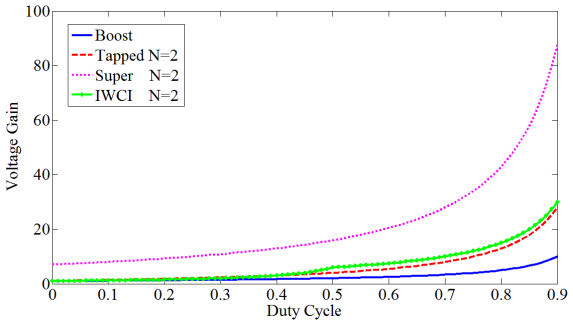


Figure 5.35. Voltage-gain comparison of the selected converters.

Figure 5.35 shows that the super tapped-inductor converter with voltage multiplier capacitors offers the highest voltage-gain in comparison to the other selected converters. This ideal voltage-gain is much higher than the conventional boost converter and almost four times the voltage-gain of the IWCI and Tapped-inductor converters (for the case of a duty cycle of 0.9) This converter offers an outstanding performance in all the duty cycle range. Moreover, the IWCI high step-up converter presents higher voltage-gain than the tapped-inductor and the conventional boost converter, especially when the duty cycle is higher than 0.5.

Nevertheless, it is necessary to take into account that the super tapped-inductor converter with voltage multiplier capacitors has more additional components than the IWCI or the tapped-inductor converters.

In this context, in order to have a fair and more realistic comparison of the selected converters, the parasitic resistance effect must be considered. Therefore, Figure 5.36 presents the non-deal voltage-gain of the four selected converters evaluated with $N=2$ and $R_L/R_o=0.001$ ($R_L=R_{L1}$ for the tapped inductors).

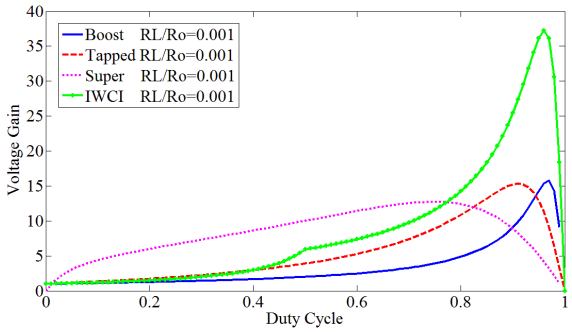


Figure 5.36. Non-ideal voltage-gain comparison of the selected converters.

Figure 5.36 shows a great drawback of the super tapped-inductor converter. Although it presents the highest ideal voltage-gain, the presence of many components and the location of the tapped-inductor prior the boosting and switched capacitors produces that the parasitic resistances deteriorate the voltage-gain. Consequently, the voltage-gains for duty cycles higher than 0.75 decrease rapidly.

In addition, it is evident the outstanding voltage-gain of the IWCI converter, i.e., it achieves much higher voltage-gain than the other converters at duty cycles higher than 0.75.

From these results, IWCI converter offers suitable characteristics of high voltage-gain, relatively simple in its construction, and a few additional components. Therefore, it is possible to state that IWCI converter is a promising topology to be applied in electric mobility applications.

5.7 Magnetic Flux Modeling

This section addresses the modeling of magnetic flux in the core of the novel coupled inductor. This analysis is essential in order to clarify the advantages of the proposed converter, understand the downsizing design of the magnetic core, and illustrate the non-triangular flux behavior that the coupled inductor presents. Moreover, these discussions can give a better understanding of the performance of magnetic structures with different magnetic flux waveforms.

The analysis of the magnetic characteristics of the coupled inductor used for this particular HSU converter is conducted taking into account the magnetic circuit model and the operating principle. Figure 5.13 shows the magnetic circuit for the integrated coupled inductor, where R_{me} and R_{mc} correspond to the external and central reluctances of the EE core; ϕ_1, ϕ_2, and ϕ_c are the external and central magnetic fluxes, respectively; and N_e and N_c are the number of turns of the external and central windings, respectively.

Leakage fluxes are neglected in order to fully understand the effect of the additional central winding. In this context, magnetic fluxes can be divided into DC and AC components. Therefore, the magnetic flux is analyzed separately for each component.

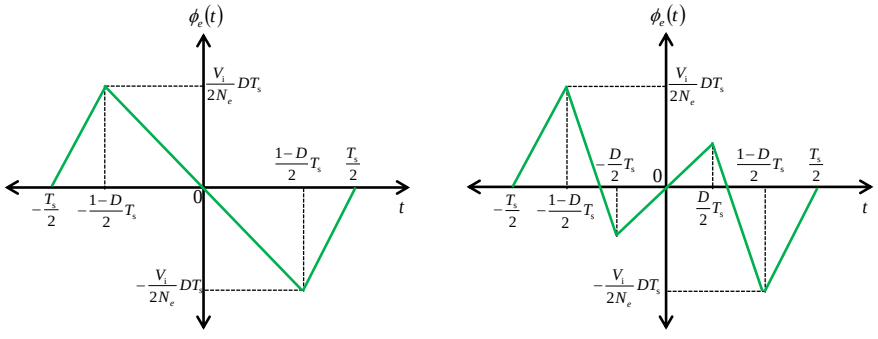
Additionally, as the DC flux is generated by the inductor average current, and the average current I_{DC} in each phase is ideally the same, the DC flux in the first external leg is equal to the one in the other external leg. This flux can be calculated from the magnetic circuit model (Figure 5.13) as $\phi_{DC}=(N_e I_{DC})/R_{me}$. In addition, as the external windings are directly coupled, the DC fluxes in the central leg, calculated as $\phi_c=\phi_1-\phi_2$, is equal to zero.

Moreover, on the basis of the Faraday's Law, applying a voltage to the inductor windings generates AC fluxes. Therefore, from Figure 5.13 and the operating modes presented in the previous sections, it is possible to deduce the AC flux equations for the external and central legs in the case of D<0.5 as follows:

Table 5.7 Winding voltage and AC flux equations when D<0.5

	Mode 1	Mode 2	Mode 3
v_{L1}	v_i	$\frac{v_i(1+N)-v_o}{1+N}$	v_i-v_o
v_{L2}	$\frac{v_i(1+N)-v_o}{1+N}$	v_i	v_i-v_o
ϕ_{AC}	$\frac{v_i}{N_e}DTs$	$\frac{v_i(N-D(1+2N))DTs}{N_e(1+N-D(1+2N))}$	$\frac{v_i(D-0.5)(1+2N)DTs}{N_e(1+N-D(1+2N))}$
ϕ_{ACc}	$\frac{v_iDTs}{N_e(1+N-D(1+2N))}$	$\frac{-v_iDTs}{N_e(1+N-D(1+2N))}$	0

Where N is the ratio between the number of turns of the central winding to the external winding ($N=N_c/N_e$). From these equations, and taking into account the possible values of D and N, it is possible to point out that there are two possible shapes of AC flux in the external legs at D<0.5. After making a mathematical analysis of each shape, it was possible to conclude that the existence of each shape depends on the condition $N-D(1+2N)$. Therefore, the duty cycle and the turns ratio influence the flux shape at D<0.5. Figure 5.37 shows the slope of the flux at D<0.5 taking into account the condition $N-D(1+2N)$.



(a) $N-D(1+2N)<0$ (b) $N-D(1+2N)>0$

Figure 5.37. External legs flux waveforms (D<0.5).

The condition *N-D(1+2N)* (defined as a flux factor that affects the flux density) is plotted in Figure 5.38.

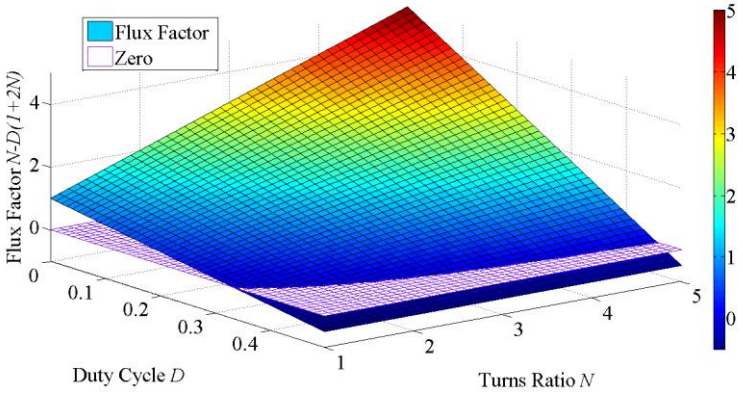


Figure 5.38. Flux factor *N-D(1+2N)*.

As seen in Figure 5.38, as most of the possible combinations of N and D are above the plane "zero", these combinations produce a non-triangular flux waveform. A triangular flux waveform is only guaranteed at duty cycles near 0.5. Also, it is possible to point out that at low turns ratios N, the range of duty cycles, where a triangular waveform is guaranteed, is increased.

Considering this behavior and the voltage gain presented when the duty cycle is lower than 0.5 [28], it is confirmed that this converter has very different operating conditions when the duty cycle is lower or higher than 0.5.

As it is known, from Faraday's law, the winding voltage is proportional to the magnetic flux variations and the number of turns. In the same way, the winding currents are dependent on the magnetic reluctances, the number of turns, and the magnetic flux. Consequently, knowing the possible shapes of the magnetic flux and the issues that influence these shapes, the designers can have more criteria that may be helpful for choosing the suitable operating point based on their requirements.

On the other hand, the AC flux equations for the case of D>0.5 are presented as follows:

Table 5.8 Winding voltage and AC flux equations when D>0.5

	Mode 1	Mode 2	Mode 4
v_{L1}	v_i	$\frac{v_i(1+N)-v_o}{1+N}$	v_i
v_{L2}	$\frac{v_i(1+N)-v_o}{1+N}$	v_i	v_i
ϕ_{AC}	$\frac{v_i}{N_e}(1-D)Ts$	$-\frac{v_i}{N_e}DTs$	$-\frac{v_i}{N_e}(D-0.5)Ts$
ϕ_{ACc}	$\frac{v_i}{N_e}DTs$	$-\frac{v_i}{N_e}DTs$	0

Based on these equations, the waveform of the AC fluxes in the external legs at D>0.5 is shown in Figure 5.39.

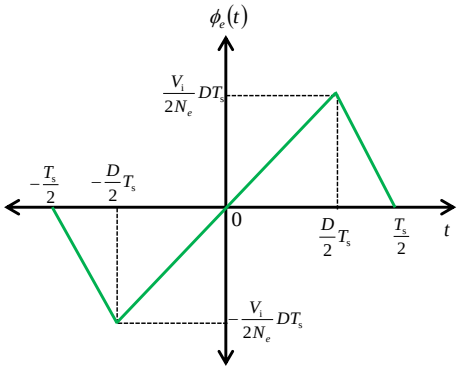
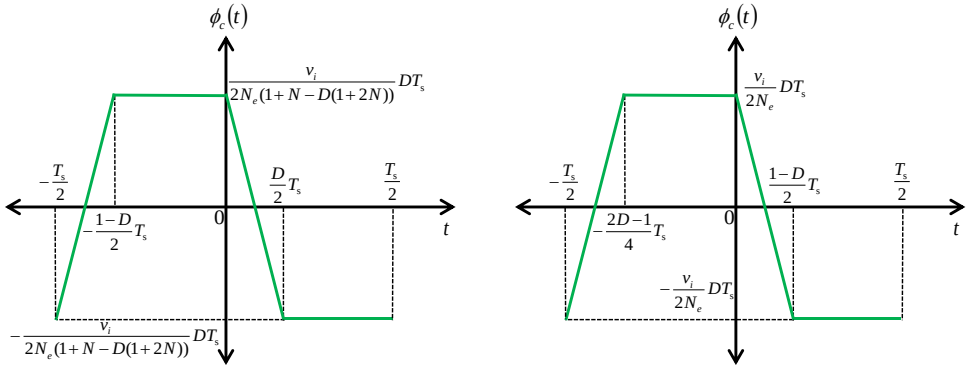


Figure 5.39. External legs flux waveform (D>0.5).

Now, considering the AC flux in each external leg, it is possible to calculate the AC flux through the central leg. Figure 5.40 shows the waveforms of the AC flux in the central leg for both duty cycle cases.



(a) D<0.5 (b) D>0.5

Figure 5.40. Central leg flux waveforms.

Finally, using the DC and AC fluxes, the peak flux equations can be calculated as follows:

$$\phi_{peak-e} = \frac{N_e I_{DC}}{R_{me}} + \frac{V_i}{2N_e} DT_s \tag{5.72}$$

$$\phi_{peak-c-D<0.5} = \frac{V_i}{2N_e(1+N-D(1+2N))} DT_s \tag{5.73}$$

$$\phi_{peak-c-D>0.5} = \frac{V_i}{2N_e} DT_s \tag{5.74}$$

With the derivation of the peak flux, the design of the inductor based on the maximum magnetic flux allowed by the selected core can be conducted, as well as the core size and the downsizing analysis can be addressed.

5.7.1 Validation

In order to validate and to have a better understanding of the effect of magnetic integration on HSU DC-DC converters, a 1kW circuit of the analyzed converter was simulated in PLECS. This circuit was simulated with a turns ratio of two, 200V of output voltage, and an input voltage between the range of 20V and 152V, in order to evaluate different conversion ratios and different values of duty cycle. In addition, the simulations were set at 1 kW of output power and 30 kHz of switching frequency. Figure 5.41 shows the schematics of the simulated circuit.

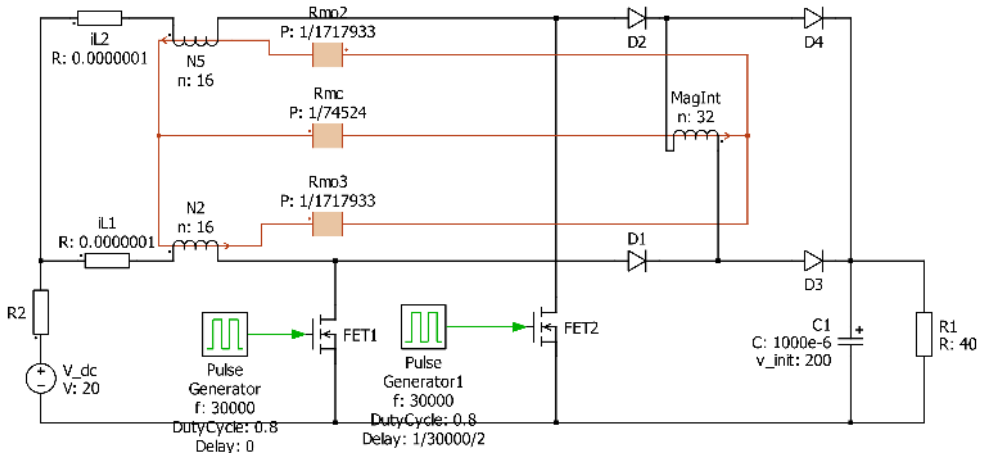


Figure 5.41. Simulated circuit.

Figure 5.42 and Figure 5.43 present the simulated waveforms for both duty cycle cases. In each figure, winding currents, magnetic fluxes, and gate signals are provided. Figure 5.42 shows the non-triangular flux waveform at D=0.27. With these waveforms, the analysis presented above is validated because the simulations present the same shape of the modeling theory.

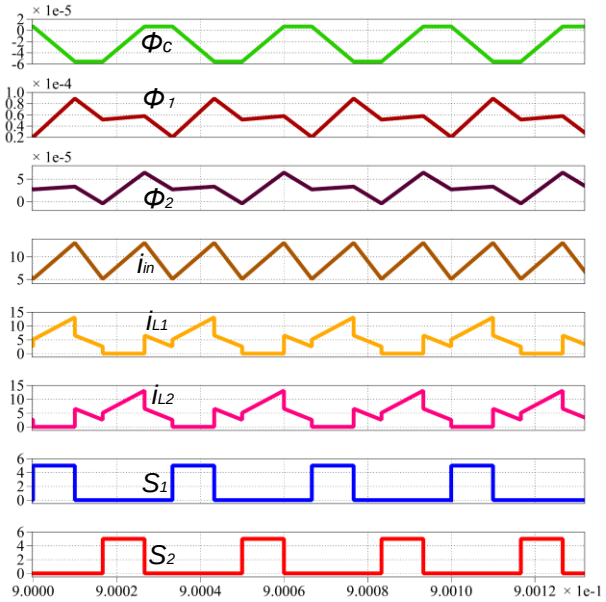


Figure 5.42. Simulation results at D=0.27 (D<0.5).

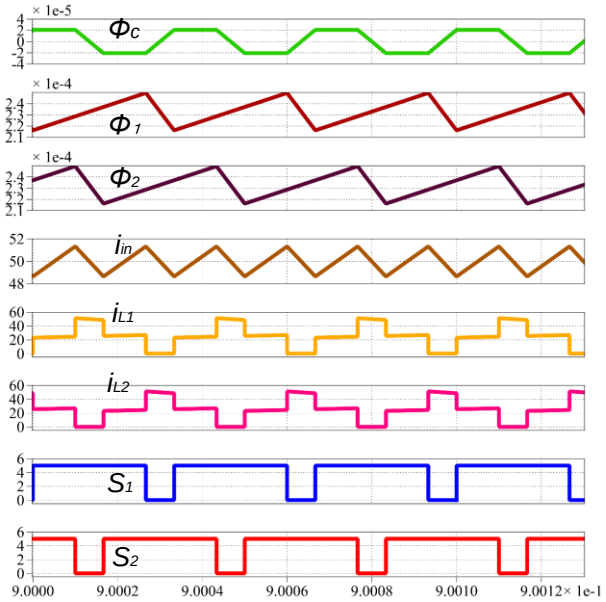
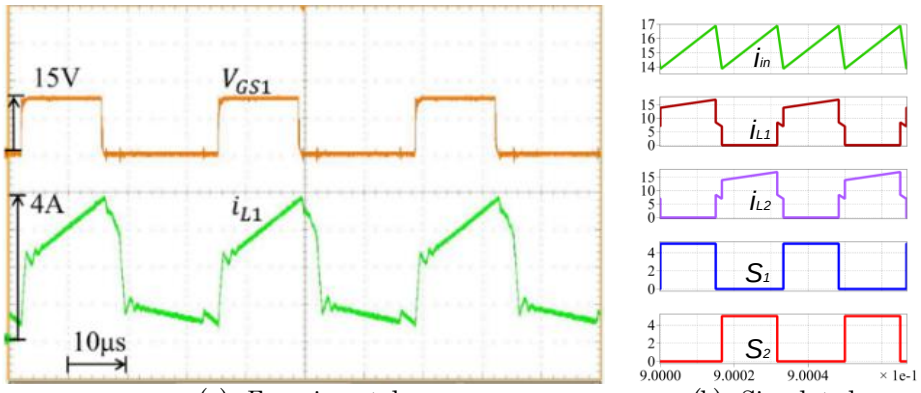


Figure 5.43. Simulation results at D=0.8 (D>0.5).

Finally, experimental tests of a 1kW prototype were conducted. Figure 5.44 shows the measured gate-source voltage and one of the winding currents. In addition, Figure 5.44 shows the simulated currents at the same duty cycle of the measurements in order to see the validation.



(a) Experimental (b) Simulated

Figure 5.44. Experimental and simulated waveforms.

5.8 Conclusions

A novel high step-up two-phase interleaved boost converter with a particular coupled-inductor was evaluated in this section from different point of views. First, the circuit configuration and the operating principle were presented as the base of the steady-state analysis where it was possible to calculate the voltage-gain performance of the analyzed converter.

Second, two different configurations of coupled-inductor were evaluated. A performance comparison was conducted to evaluate the effectiveness of the integrated coupled-inductor in comparison to the two cores coupled-inductor. The integrated coupled-inductor was found to exhibit a voltage-gain 20% higher than the two cores coupled-inductor when the converter is operating at a duty cycle of 80% and a ratio of turns of 2. In addition, the proposed converter offers a reduction of the input current ripple in comparison to the conventional interleaved boost converter.

Third, a parasitic analysis of the proposed converter was conducted. It was found that the voltage-gain is reduced when the parasitic resistance is increased. In addition, it was found that the parasitic resistance affects largely as the ratio of the number of turns in the integrated magnetic component in the proposed converter increases and particularly when the duty cycle is larger than 0.5. However, its voltage conversion ratio is higher than the conventional topologies. Finally, efficiency experimental tests were conducted and it was found that the efficiency decreases when the parasitic resistance increases.

Fourth, the voltage-gain of four outstanding high step-up converters that are promising to be applied in electric mobility applications was presented. This study is performed on the base of the operating principle of conventional two-phase interleaved boost converters with coupled-inductors, which integrate the techniques of interleaving phases and magnetic integration. These techniques have been reported as effective to downsize power converters and therefore to be applied in EV applications. From the comparative analysis of the selected topologies, it was possible to conclude that the converters that offer the best

relative performance in terms of a few number of components are the tapped-inductor and the IWCI high step-up converters. It was also found that the super tapped-inductor converter with voltage multiplier capacitors offers the highest ideal voltage-gain in all the duty cycle range. In addition, IWCI converter offers higher voltage-gain than the tapped-inductor and the conventional boost converters.

However, once the parasitic effects are considered, the super tapped-inductor presents a considerable voltage-gain reduction, making it comparable to the other topologies. And at high duty cycles, its voltage-gain becomes smaller than the other converters. Moreover, the IWCI converter presents a quite outstanding operation at D>0.75 offering the highest voltage-gain in comparison to the selected converters.

Fifth, the magnetic flux of the coupled inductor was modeled as well. As a result, it was found that the coupled inductor exhibits a non-triangular flux waveform when the duty cycle is lower and close to 0.5. In addition, the peak magnetic fluxes on the external and central legs were derived. These models are the base for the design and downsizing of the coupled inductor. Moreover, these results can be a guide for magnetic and electrical characterization of different high step-up converters.

Finally, taking into account the evaluation of number of components, ideal and non-ideal voltage-gain of the compared topologies, it is possible to conclude that the IWCI converter, proposed by the authors, is a suitable combination between high voltage-gain and number of components, and thereby it is a promising topology to be applied in electric mobility applications.

Taking into account the advantages of the proposed converter in terms of voltage-gain and number of additional components, it is possible to conclude that it is a promising topology for renewable energies and electric vehicles applications when a high conversion ratio and high power density are required

References

[1] K. Park, G. Moon and M. Youn, "Nonisolated High Step-Up Stacked Converter Based on Boost-Integrated Isolated Converter," *IEEE Transactions on Power Electronics,* Vol. 26, no.2, pp.577-587. 2011.

[2] W. Li, J. Liu, J. Wu and X. He, "Design and Analysis of Isolated ZVT Boost Converters for High-Efficiency and High-Step-Up Applications," *IEEE Transactions on Power Electronics,* Vol. 22, no. 6, pp. 2363-2374, 2007.

[3] W. Martinez, J. Imaoka, Y. Itoh, M. Yamamoto and K. Umetani, "Analysis of Coupled-Inductor Configuration for an Interleaved High Step-Up Converter," *IEEE International Conference on Power Electronics – ICPE 2015-ECCE Asia,* pp. 2591-2598, 2015.

[4] R. Gules, L. Pfitscher and L. Franco, "An Interleaved Boost DC-DC Converter with Large Conversion Ratio," *IEEE International Symposium on Industrial Electronics, ISIE*, pp. 411-416, 2003.

[5] W. Martinez, J. Imaoka, M. Yamamoto and K. Umetani. "Parasitic Resistance Analysis in a Novel High Step-Up Interleaved Converter for Hybrid Electric Vehicles", *Journal of the Japan Institute of Power Electronics* ISSN: 1884-3239, vol. 40, no. 1, pp. 93-104, Mar, 2015.

[6] W. Martinez, J. Imaoka, Y, Itoh, M. Yamamoto and K. Umetani "A Novel High Step-Down Interleaved Converter with Coupled Inductor," *IEEE International Telecommunications Energy Conference - INTELEC*, pp. 1-6, 2015.

[7] W. Li, X. Xiang, C. Li, W. Li and X. He, "Interleaved High Step-Up ZVT Converter with Built-In Transformer Voltage Doubler Cell for Distributed PV Generation System," *IEEE Transactions on Power Electronics,* Vol. 28, no. 1, pp. 300-313, 2011.

[8] W. Li, W. Cui, Y. Zhao, B. Yang, and X. He, "Interleaved high step-up converter with built-in transformer and voltage doubler for PV grid-connected generation systems," *European Conference on Power Electronics and Applications (EPE 2011)*, pp. 1-10, 2011.

[9] J. Fangjian, K. Shin: "Pack Sizing and Reconfiguration for Management of Large-Scale Batteries", *IEEE/ACM Third International Conference on Cyber-Physical Systems (ICCPS)*, pp. 138-147, 2012.

[10] W. Martinez, J. Imaoka, S. Kimura, M. Yamamoto and C. Cortes, "Volume Comparison of DC-DC Converters for Electric Vehicles," *IEEE Workshop on Power Electronics and Power Quality Applications - PEPQA,* pp. 1-6, 2015.

[11] K. Taesic, Q and Wei, Q. Liyan: "A multicell battery system design for electric and plug-in hybrid electric vehicles", *EEE International Electric Vehicle Conference (IEVC)*, pp. 1-7, 2012.

[12] W. Martinez, C. Cortes and L. Munoz, "Sizing of Ultracapacitors and Batteries for a High Performance Electric Vehicle," *IEEE International Electric Vehicle Conference – IEVC*, pp. 535-541, 2012.

[13] S. Bashash, S. Moura, and H. Fathy, "Charge trajectory optimization of plug-in hybrid electric vehicles for energy cost reduction and battery health enhancement," *American Control Conference (ACC)*, pp. 5824-5831, 2010.

[14] J. Imaoka, S. Kimura, Y. Itoh, M. Yamamoto, M Suzuki and K. Kawano, "Feasible evaluations of coupled multilayer chip inductor for POL converter," *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA)*, pp. 883-890, 2014.

[15] M. Hirakawa, M. Nagano, Y. Watanabe, K. Andoh, S. Nakatomi and S. Hashino, "High Power Density DC/DC Converter using the Close-Coupled Inductors," *1st IEEE Energy Conversion Congress and Exposition (ECCE),* pp.1760-1767. 2009.

[16] W. Martinez and C. Cortes, "High Power Density Interleaved DC-DC Converter for a High Performance Electric Vehicle", *IEEE Workshop on Power Electronics and Power Quality – PEPQA*, pp. 1-6, 2013.

[17] G. Calabrese, M. Granato, G. Frattini, and L. Caprineri, "Integrated Gate Drive Architecture for High Step-down Multiphase Buck Converter," *International Exhibition and Conference for Power Electronics PCIM Europe,* pp. 1-8, 2015.

[18] S.V. Araujo, R. P. T. Bascope, G. V. T. Bascope and L. Menezes, "Step-Up Converter with High Voltage-gain Employing Three-State Switching Cell and Voltage Multiplier," *Proc. IEEE Power Electron. Specialists Conf. (PESC)*, pp. 2271-2277, 2008.

[19] K. Pavlovsky, G. Guidi and A. Kawamura, "Assessment of Coupled and Independent Phase Designs of Interleaved Multiphase Buck/Boost DC–DC Converter for EV Power Train," *IEEE Transactions on Power Electronics*, vol.29, no.6, pp.2693-2704. 2014.

[20] K. Umetani, J. Imaoka, M. Yamamoto, A. Seikoh and T. Hirano, "Evaluation of the Lagrangian method for deriving equivalent circuits of integrated magnetic components: A case study using the integrated winding coupled inductor," *IEEE Energy Conversion Congr. Expo. (ECCE2013)*, pp. 495-502. 2013.

[21] K. Hartnett, J. Hayes, M. Egan, and M. Rylko: "CCTT-Core Split-Winding Integrated Magnetic for High-power DC-DC Converters", *IEEE Transactions on Power Electronics*, vol.28, pp.4970-4984, 2013.

[22] P. Wong, P. Xu, B. Yang and F. C. Lee: "Performance Improvements of Interleaving VRMs with Coupling Inductors", *IEEE Transactions on Power Electronics*, vol.16, no.4, pp.499-507, 2001.

[23] J. Imaoka, M. Yamamoto, K. Umetani, S. Arimura, and T. Hirano, "Characteristics analysis and performance evaluation for interleaved boost converter with integrated winding coupled inductor," *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.3711-3718. 2013.

[24] S. Dwari and L. Parsa. "An Efficient High-Step-Up Interleaved DC–DC Converter with a Common Active Clamp," *IEEE Transactions on Power Electronics*, vol.26, no.1, pp.66-78, 2011.

[25] W. Li, W. Li and X. He, "Zero-voltage transition interleaved high step-up converter with built-in transformer," IEEE Transactions on Power Electronics, Vol.4, no.5, pp.523-531, 2011.

[26] Z. Shi, K. Cheng, and S. Ho, "Static performance and parasitic analysis of tapped-inductor converters," IET Power Electronics, 7(2), 366-375. 2014.

[27] K. Tseng, C. Ou, Hang, and C. Cheng, "A Single-Switch Converter with High Step-up Gain and Low Diode Voltage Stress Suitable for Green Power-Source Conversion," IEEE Journal of Emerging and Selected Topics in Power Electronics, PP(99),1. 2015.

[28] W. Martinez, J. Imaoka, Y. Itoh, M. Yamamoto and K. Umetani, "Analysis of Coupled-Inductor Configuration for an Interleaved High Step-Up Converter," *IEEE International Conference on Power Electronics – ICPE 2015-ECCE Asia*, pp. 2591-2598, 2015.

6. Conclusions

Integrated magnetics is an outstanding technique capable to be applied to power converters in order to achieve high power density performance through the downsizing of magnetic components by the integration of several windings into only one core. Therefore, in this document, magnetic integration was studied for those applications where non-isolated DC-DC converters are required. Specifically, it was expected that this technique helped tackle three specific issues of the power converters aimed to be applied to electric mobility applications: 1. Low power density, i.e., high mass and large volume of the electric systems. 2. Low efficiency. And, 3. Low voltage gain.

This document addressed these issues by proposing a study of several non-isolated DC-DC converters, mainly most of them proposed by the author.

Chapter 2 presented a volume modeling methodology of four DC-DC converter topologies, combining geometry sizing, inductor modeling, power loss evaluation, and heat sinks modeling of conventional and next-generation devices. With this analysis, the power density of several topologies with magnetic integration were evaluated. Moreover, a novel approach to increase the efficiency was presented (the Short-Circuited Winding).

Chapter 3 presented a novel single-phase recovery-less boost converter with saturable inductors. In addition, the interleaved two-phase recovery-less converter was proposed as well. These two topologies that use the concept of magnetic integration were studied for their capability to increase the efficiency by reducing the reverse recovery phenomenon.

Chapter 4 showed a novel high step-down two-phase interleaved buck converter with a particular coupled-inductor. This coupled-inductor integrates three windings into only one core offering the characteristic of a high step-down conversion ratio.

Finally, chapter 5 presented an analysis of the novel high step-up two-phase interleaved boost converter with a particular coupled-inductor from different point of views: Evaluation of two arrangements of coupled-inductor, comparison with other high step-up converters, derivation of voltage gain with parasitic components and the comparison with non-ideal voltage gains of other converters.

From these analyses of several converters, it is possible to conclude that magnetic integration technique is a powerful technique capable of dealing with the issues mentioned above for high demanding applications like renewable energies or electric mobility.

Publications

This is a summary of the publication products of this research.

Transactions

[1] **W. Martinez,** J. Imaoka, M. Yamamoto and K. Umetani, "Parasitic Resistance Analysis in a Novel High Step-Up Interleaved Converter for Hybrid Electric Vehicles," *Journal of the Japan Institute of Power Electronics ISSN: 1884-3239,* vol. 40, no. 1, pp. 93-104, Mar, 2015.

[2] **W. Martinez,** J. Imaoka, K. Nanamori, M. Yamamoto and T. Kawashima, "Recovery-Less Boost Converter with Saturable Inductor for Electric Vehicle Applications," *IEEJ Transactions on Industry Applications ISSN: 1348-8163,* vol. 135, no, 9. pp, 914-921 Sep. 2015.

Transactions as co-author

[3] J. Imaoka, **W. Martinez,** S. Kimura, and M. Yamamoto, "A Novel Integrated Magnetic Core Structure Suitable for Transformer-linked Interleaved Boost Chopper Circuit," *IEEJ Journal of Industry Applications ISSN: 2187-1108*, vol.3, no.5, pp. 395-404, Sep. 2014.

[4] J. Imaoka, S. Kimura, Y. Itoh, **W. Martinez,** M. Yamamoto, M. Suzuki and K. Kawano, "Feasible Evaluations of Coupled Multilayer Chip Inductor for POL Converters," *IEEJ Journal of Industry Applications ISSN: 2187-1108*, vol. 4, no, 3, pp. 126-135, May. 2015.

[5] J. Imaoka, **W. Martinez** and M. Yamamoto, "Coupling Coefficient Improvement and Electromagnetic Induced Noise Reduction using Short-Circuited Winding for Loosely Coupled Inductor," *IEEJ Journal of Industry Applications*, vol. 5, no, 2, pp. 174-175, Feb. 2016.

[6] J. Imaoka, K. Umetani, S. Kimura, **W. Martinez**, M. Yamamoto, S. Arimura and T. Hirano, "Magnetic Analysis, Design and Experimental Evaluations for Integrated Winding Coupled Inductor in Interleaved Converters," *IEEJ Journal of Industry Applications*, vol. 5, no. 3, 276-288, May 2016.

[7] S. Kimura, Y. Itoh, J. Imaoka, **W. Martinez** and M. Yamamoto, "Downsizing Effects of Integrated Magnetic Components in High Power Density DC-DC Converters for

EV and HEV," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, 3294 - 3305, Jul 2016.

Conference Papers

[1] **W. Martinez**, S. Kimura, J. Imaoka, M. Yamamoto, K. Umetani, T. Hirano and S. Arimura, "High Power Density DC-DC Converter for Home Energy Management Systems," *IEEE International Green Building and Smart Grid Conference - IGBSG*, pp. 1-6, Taipei-Taiwan, Apr, 2014. *Invited Paper*.

[2] **W. Martinez**, M. Yamamoto, P. Grbovic and C. Cortes, "Efficiency Optimization of a Single-Phase Boost DC-DC Converter for Electric Vehicle Applications," *IEEE 40th Annual Conference of the IEEE Industrial Electronics Society – IECON*, pp. 4279-4285, Dallas-USA, Oct, 2014.

[3] **W. Martinez**, J. Imaoka, Y. Itoh, M. Yamamoto and K. Umetani, "Analysis of Coupled-Inductor Configuration for an Interleaved High Step-Up Converter," *IEEE International Conference on Power Electronics – ICPE 2015-ECCE Asia,* pp. 2591-2598, Seoul-Korea, Jun, 2015.

[4] **W. Martinez**, J. Imaoka, S. Kimura, M. Yamamoto and C. Cortes, "Volume Comparison of DC-DC Converters for Electric Vehicles," *IEEE Workshop on Power Electronics and Power Quality Applications-PEPQA*, pp. 1-6, Bogota-Colombia, Jun, 2015.

[5] **W. Martinez**, J. Imaoka and M. Yamamoto, "ZCS Interleaved Boost Converter with Saturable Inductors for Reverse-Recovery Reduction," *IEEE International Conference on Power Electronics and Drive Systems-PEDS,* pp. 855-861, Sydney-Australia, Jun, 2015.

[6] **W. Martinez**, J. Imaoka and M. Yamamoto, "Analysis of Output Capacitor Voltage Ripple of the Three-Phase Transformer-Linked Boost Converter," *IEEE 17th Conference on Power Electronics and Applications, EPE'15-ECCE Europe*, pp. 1-9, Geneva-Switzerland, Sep, 2015.

[7] **W. Martinez**, J. Imaoka, Y, Itoh, M. Yamamoto and K. Umetani "A Novel High Step-Down Interleaved Converter with Coupled Inductor," *IEEE International Telecommunications Energy Conference - INTELEC*, pp. 1-6, Osaka-Japan, Oct, 2015.

[8] **W. Martinez**, J. Imaoka, S. Kimura, M. Yamamoto and C. Cortes, "Volume Comparison of DC-DC Converters for Electric Vehicles," *IEEE IAS Annual Meeting*, poster, Dallas, TX-USA, Oct, 2015. *Invited Poster*

[9] **W. Martinez**, J. Imaoka, M. Yamamoto and K. Umetani "High Step-Up Interleaved Converter for Renewable Energy and Automotive Applications," *IEEE International Conference on Renewable Energy Research and Applications - ICRERA*, pp. 1-6, Palermo-Italy, Nov, 2015.

[10] **W. Martinez**, M. Yamamoto, J. Imaoka, F. Velandia and C. Cortes, "Efficiency Optimization of a Two-Phase Interleaved Boost DC-DC Converter for Electric Vehicle Applications," *IEEE International Conference on Power Electronics – IPEMC 2016-ECCE Asia*, pp. 1-7, Hefei China, May, 2016.

[11] **W. Martinez**, M. Noah, M. Yamamoto, and J. Imaoka, "Reverse-Recovery Current Reduction in a ZCS Boost Converter with Saturable Inductors using Nanocrystalline Core Materials," *IEEE 18th Conference on Power Electronics and Applications, EPE'16-ECCE Europe*, pp. 1-9, Karlsruhe-Germany, Sep, 2016.

[12] **W. Martinez**, M. Noah, M. Yamamoto, and J. Imaoka, "Three-Phase LLC Resonant Converter with Integrated Magnetics," *IEEE Energy Conversion Congress and Exposition- ECCE*, pp. 1-8, Milwaukee-USA, Sep, 2016.

Conference Papers as co-authors

[13] A. Nishigaki, **W. Martinez**, H. Umegami, F. Hattori and M. Yamamoto "An Analysis of False Turn-On Mechanism on Power Devices," *IEEE Energy Conversion Congress and Exposition-ECCE*, pp. 2988-2993, Pittsburg-USA, Sep, 2014.

[14] H. Ishibashi, **W. Martinez**, A. Nishigaki, H. Umegami, and M. Yamamoto, "An analysis of false turn-on mechanism on high-frequency power devices," *IEEE Energy Conversion Congress and Exposition- ECCE*, pp. 2247-2253, Montreal-Canada, Sep, 2015.
[15] M. Ishihara, **W. Martinez**, S. Kimura and M. Yamamoto, "Analysis and design of passive components for interleaved flyback converter with integrated transformer," *IEEE Energy Conversion Congress and Exposition- ECCE*, pp. 5902-5909, Montreal-Canada, Sep, 2015.
[16] F. Velandia, **W. Martinez**, C.A. Cortes, M. Noah and M. Yamamoto, "Power Loss Analysis of Multi-Phase and Modular Interleaved Boost DC-DC Converters with Coupled Inductor for Electric Vehicles," *IEEE 18th Conference on Power Electronics and Applications, EPE'16-ECCE Europe*, pp. 1-9, Karlsruhe-Germany, Sep, 2016.
[17] D. Ebisumoto, J. Imaoka, Y. Ito, **W. Martinez**, M. Ishihara, S. Aoto and M. Yamamoto, "A Magnetic Structure of Coupled-Inductor Suitable for a Four-Phase Interleaved Boost Converter with Phase Drive Control," *IEEE Energy Conversion Congress and Exposition- ECCE*, pp. 1-8, Milwaukee-USA, Sep, 2016.

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