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The Present Status and Prospects in GaAs-on-Si Electronic Devices

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Abstract

Power metal semiconductor field effect transistors (MESFET's) have been fabricated to show that they have come to the stage of practical use. This paper reviews what have inhibited the practical use of GaAs-on-Si electronic devices and how they have been overcome by focusing the application of GaAs-on-Si to the power MESFET's and high electron mobility transistors (HEMT's). It is demonstrated that the practical application of the GaAs-on-Si power MESFET's to the base–station devices for mobile phones is one of the most attractive in the very near future.

1. Introduction

Since the innovation of heteroepitaxial growth of GaAs on Si in 1984[1,2], various applied devices have been fabricated on GaAs-on-Si wafers[3–5], but three main inherent problems, the dislocations, surface roughness and parasitic capacitances have inhibited the practical application of GaAs-on-Si wafers. Most of the forerunners quitted researches on GaAs-on-Si devices because of theses problems. However, recently it has been found that these difficulties have been overcome provided that GaAs-on-Si wafers are applied to suitable electronic devices[6–9].

In high electron mobility transistor (HEMT) all-epitaxially fabricated on Si, remarkably small scatter in the threshold voltage distribution (σVth) has been obtained and the dislocation densities are found to be unrelated to the Vth inhomogeneities. In addition, recent developments in fabrication and analysis, using small signal equivalent circuits for HEMT's and power metal semiconductor transistors (MESFET's) on Si, have shown that the parasitic capacitances arise from the interface carriers generated by the autodiffusion of Si into GaAs at the GaAs–Si interface and that the influence on the high frequency performance of these devices can be greatly reduced by minimizing the pad capacitances.

In this paper the experimental results mainly obtained by the present author and co-workers are reviewed in detail and the prospects of the GaAs-on-Si electron devices are discussed on the basis of the present state of the arts in these devices.

2. Preparation of GaAs/Si wafers

The epitaxial layers of GaAs and/or GaAlAs were grown by metalorganic chemical vapor deposition (MOCVD), using a vertical type apparatus with a high speed rotating substrate system. The growth procedures consist of the conventional two-step method for GaAs growth on a Si substrate using trimethylgallium (TMG), trimethylaluminum (TMA) and arsine (AsH_3). The growth temperature is 650°C. Doping is carried out with disilane (Si_2H_4) and the total pressure is 60 Torr. Although dielectric film coating for Si backside is not carried out, it is indicated from capacitance-voltage measurement that vaporized Si atoms from the substrate are not included in the epitaxial layer, which is an advantage for the present MOCVD system compared to a horizontal-type system suffering from the inclusion of Si atoms. The Si (100) substrates are 3 inches in diameter and misoriented by 3° toward [011].

Etch pit densities of the as-grown GaAs/Si are observed to be over the order of 10^7 cm^{-2} by molten KOH etching and cross-sectional transmission electron microscopy (TEM).

It has been reported that surface morphology for the GaAs/Si, namely surface roughness and surface pits, induced the device failure during the fabrication process.

From atomic force microscopy (AFM) observation, it is indicated that a value of root mean square for surface roughness for the present as-grown GaAs/Si is as small as 3.5 nm in a 50×50 μm^2 area and there are no longer pits. Furthermore, the X-ray rocking curves yield a full width half maximum (FWHM) of 200 arc-sec for the GaAs/Si. Comparing these results with those reported, it is found that the present GaAs/Si has the high quality both crystallographically and morphologically.

3. Effect of dislocations on the Vth uniformity

3.1 HEMT on Si

HEMT structures used here consist of a 1.5 μm thick GaAs buffer layer, a 1.5 μm thick AlGaAs buffer layer, a 0.05 μm thick GaAs channel layer, a 0.05 μm thick doped AlGaAs layer and a 0.1 μm thick doped GaAs cap layer. Carrier concentration of the doped AlGaAs is varied from 7.0 to 12.0×10^{17} cm^{-3} and that of the doped GaAs is 1.5×10^{18} cm^{-3}. The Al content in the AlGaAs layer is 0.25. The device fabrication processes are carried out using mesa chemical etching, conventional photolithography, AuGe/Ni evaporation for gates after GaAs/AlGaAs selective dry etching.

Fig. 1 shows typical current-voltage characteristics for the depletion mode HEMT/Si with a doping concentration of the doped AlGaAs of 9.5×10^{17} cm^{-3}. The gate length and the width are 0.8 μm and 20 μm, respectively. The pinch-off characteristics and the maximum transconductance of 200 mS/mm are almost the same as those for HEMT/GaAs. Moreover, there is no difference in the characteristics between the middle- and high-resistivity Si substrate.

In order to evaluate the influence of dislocations on the threshold voltage (Vth) uniformity, a microscopic evaluation as well as a macroscopic (full wafer) evaluation is carried out, because the microscopic evaluation can reveal the influence of the dislocations on Vth under the

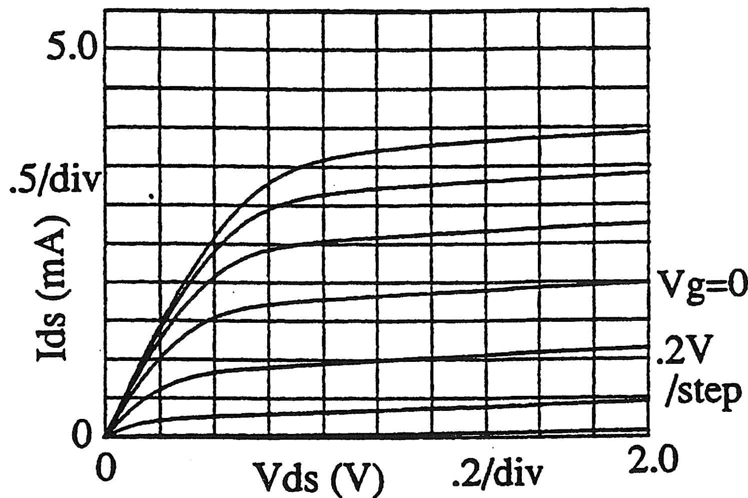

Fig. 1 A typical current-voltage characteristic for a depletion mode HEMT fabricated on Si (HEMT/Si).

condition without the fluctuation of carrier concentration and layer thickness in a wafer and of fabrication process. In the macroscopic evaluation, 200–250 HEMT's uniformly distributed in a 3-inch wafer are measured. The microscopic evaluation is carried out using 150 HEMT's distributed in a 1.95×1.90 mm^2 area. The gate length is 1.2 μm and the width is 20 μm for the macroscopic and 30 μm for the microscopic evaluation. Vth values are determined at a drain bias of 2.0 V.

The macroscopic evaluation carried out for the as-grown HEMT's/Si shows standard deviation of Vth(σVth) of 36 mV with Vth of -2.41 V for the depletion and σVth of 31 mV with Vth of 0.01 V for the enhancement mode, respectively. Fig. 2 shows the Vth histograms and its distribution pattern for the as-grown HEMT's/Si in the microscopic area which is located at the center of the wafer. As can be seen in Fig. 2, σVth of 9.0 mV with Vth of -0.10 V is obtained and it is comparable to that for HEMT's/GaAs. The distribution pattern also shows uniformly distributed Vth without any failures and abrupt change in Vth with the shift over 50 mV, which is contrary to the results for the ion implanted MESFET's/GaAs[10)] and the MESFET's/Si[9)].

An averaging effect brought by the high-density dislocations, however, must be also taken into account because it can make the possible influence of the dislocations on Vth undetectable and therefore, may mislead the high uniformity of Vth. The same evaluation as seen in Fig. 2 is shown in Fig. 3 for HEMT's/Si with three times of thermal annealing, which indicates σVth of 14 mV with Vth of -0.33 V and the similar distribution characteristics as shown in Fig. 2. Assuming about 10^8 cm^{-2} of the dislocations for the as-grown GaAs/Si and about 10^6 cm^{-2} for the annealed, a number of the dislocations under the gate electrode area is estimated as about 30 for the as-grown and about 0.3 for the annealed. No difference for the distribution pattern between Fig. 2 and Fig. 3 demonstrates that Vth for HEMT's/Si can not be affected by the dis-

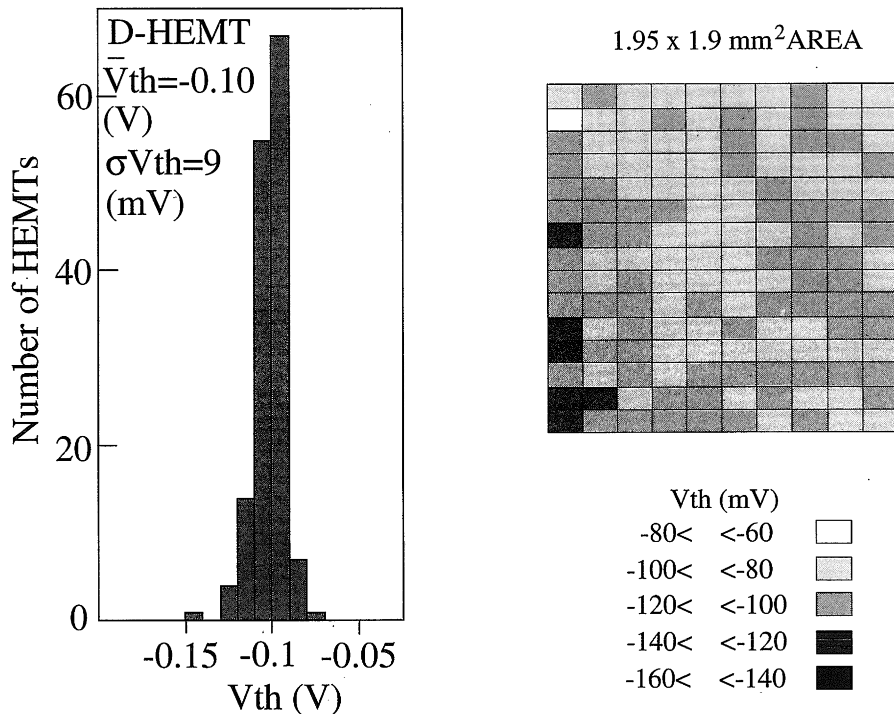

Fig. 2 Histograms and a distribution pattern of Vth for as-grown HEMT's/Si in microscopic evaluation.

locations and therefore, the high uniformity of Vth obtained for the as-grown GaAs/Si in the present study is not brought by the averaging effect. Furthermore, it should be noted that the surface morphology is indicated to be satisfactory even for the as-grown GaAs/Si from the result in Fig. 2, which show no device failures, induced during the fabrication processes.

As a conclusion for the Vth evaluation, it is more essential for obtaining high uniformity of Vth for HEMT's/Si to achieve high uniformity of doped carrier concentration and layer thickness in the wafer with good surface morphology, rather than to reduce the dislocations.

3.2 Ion-implanted GaAs/Si MESFET

A typical epilayer structure on Si, the back of which is coated with a thin SiO_2 film, used as a GaAs-on-Si substrate for the ion implantation process, consists of a 0.25 μm thick GaAs buffer layer, a 2.5 μm thick AlGaAs with an Al mole fraction of 0.25 and a hole concentration of 5×10^{16} cm^{-3}, and a 0.75 μm thick GaAs channel with an electron concentration of 7×10^{15} cm^{-3}. In order to avoid unexpected contamination throughout the FET process, a 0.25 μm thick SiO_2 film is formed by thermal oxidation, the part of which covering the mirror surface is removed prior to the MOCVD growth.

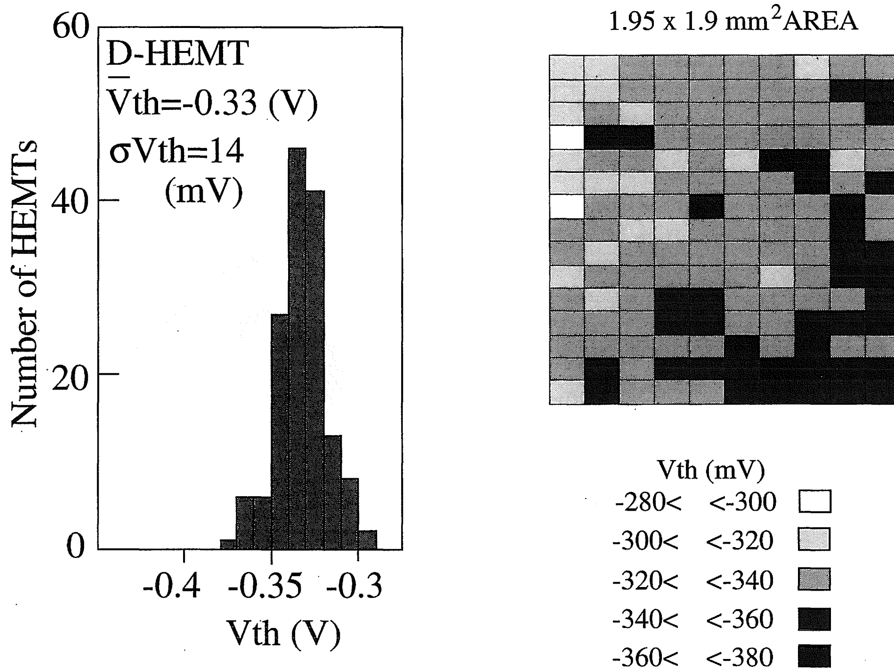

Fig. 3 Histograms and a distribution pattern of Vth for annealed HEMT's/Si in microscopic evaluation.

A stress annealing technique for obtaining low-dislocation-density regions in GaAs on Si by partially covering SiO_2 and then annealing is applied in this study. The stress annealing and subsequent FET process are schematically shown in Figs. 4(a) and 4(b) for a sectional view and a planview, respectively. An outline of the process flow is as follows. (1) A SiO_2 film about 0.4 μm thick is deposited by thermal chemical vapor deposition. (2) A 10 μm $\times$ 10 μm square area of the film for each FET is removed using buffered HF solution before the selective cap annealing. (3) Thermal cycle annealing at temperatures between 650°C to 900°C is carried out three times to give additional stress to the FET area. (4) Si ion implantation into the GaAs-on-Si wafer, as described above, is carried out using a dose of 3 to 8×10^{12} cm^{-2} at 30 keV to form the n^{++} ohmic contact layer. C ion implantation is carried out to form buried p-layers when necessary, as schematically shown in Fig. 4(a). (5) Annealing at 800°C for 20 min in AsH_3 atmosphere is made for activation. (6) W–Al metal is used as the gate electrode, which has a gate length of 0.5 to 5.0 μm and a width of 10 μm.

Five kinds of FET arrays were prepared. (A) has a buried p-layer (BP) under the channel layer on the LEC-grown GaAs wafer. (B) does not have a BP on the GaAs-on-Si wafer. (C) has a BP on the GaAs-on-Si wafer. (D) has a BP and is annealed with SiO_2 cap layer (CA) on the GaAs-on-Si wafer, (E) has a BP and selective cap annealing (SCA) is carried out.

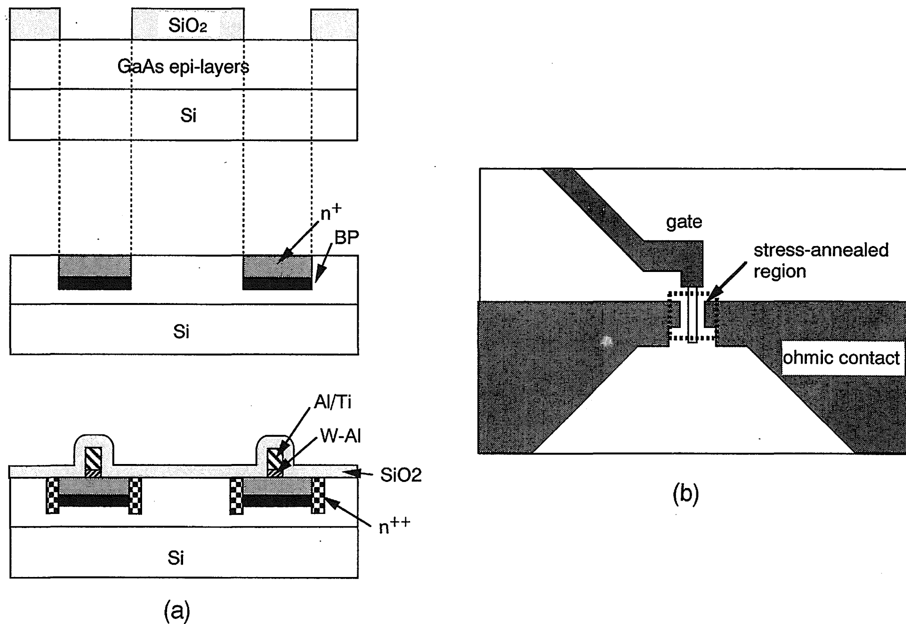

Fig. 4 (a) Cross-sectional view and (b) planview of the fabricated FET's.

The method used to measure the microscopic Vth distributions for the FET arrays is almost the same as that reported elsewhere[11]. The macroscopic Vth distribution is measured using 126 FET's distributed over the whole wafer.

The microscopic Vth distributions for samples (A), (B), (C), (D) and (E), respectively, are shown in Fig. 5 to Fig. 9. In Fig. 10, the macroscopic standard deviation of σVth-macro (●) and the microscopic standard deviation of σVth-micro (○) are shown in order to compare the samples. Fig. 5 to 10 clearly show that (1) both σVth-macro and σVth-micro decrease in the alphabetical order, indicating that buried p-layer (BP), cap annealing (CA), selective cap annealing (SCA) processes are quite effective in improving the inhomogeneity of the Vth distribution. (2) The standard deviations for sample (E) are almost comparable to those for sample (A) on GaAs. (3) In the distribution maps for the GaAs on Si wafers, no inclined patterns, referred to as cell patterns, representing the dislocations, similar to those reported for FET arrays fabricated on LEC-grown GaAs substrates are observed. (4) Although the values of σVth for samples (C) and (D) are improved by inserting the buried p-layers, some positive peaks with amplitudes of about 200 mV stand out from the background in Fig. 7 for example. More detailed examination of the electrical characteristics suggests that the positive peaks may be due to the existence of high-resistive local area in the channel layer of the FET resulting from an interaction of defects including dislocations and implanted species. We believe that the device quality resulting from SCA is high enough for devices to be utilized in small-scale integrated circuits.

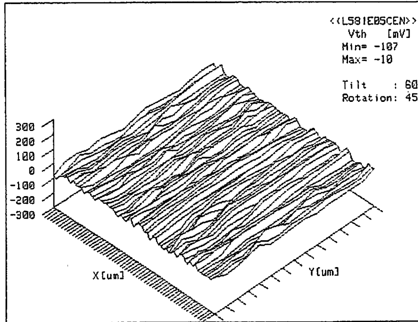

Fig. 5 Contour representation of microscopic Vth distribution for sample (A).

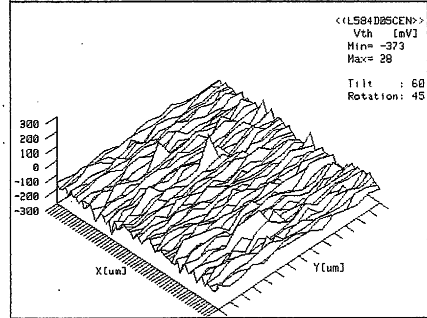

Fig. 6 Contour representation of microscopic Vth distribution for sample (B).

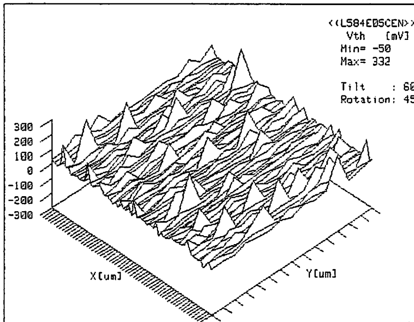

Fig. 7 Contour representation of microscopic Vth distribution for sample (C).

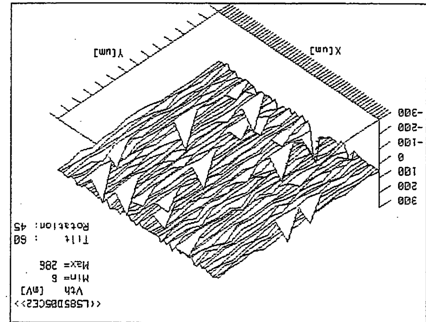

Fig. 8 Contour representation of microscopic Vth distribution for sample (D).

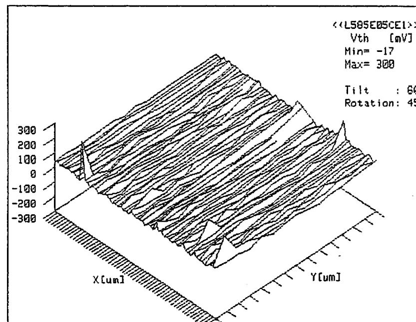

Fig. 9 Contour representation of microscopic Vth distribution for sample (E).

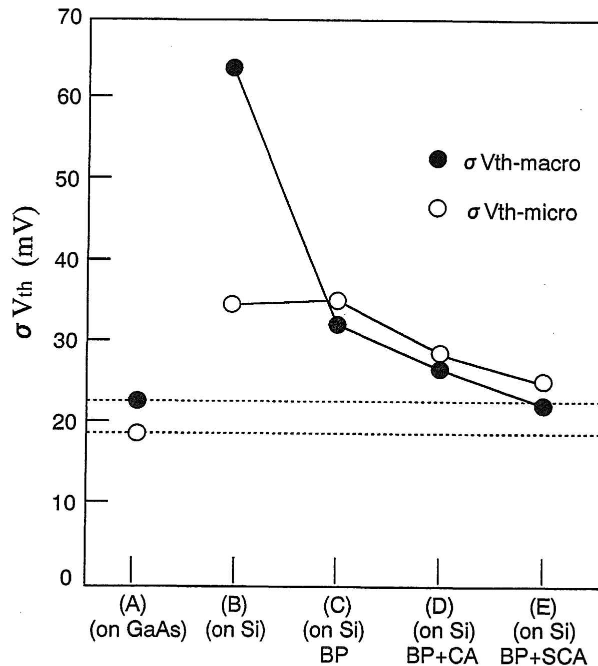

Fig. 10 σVth for samples (A)–(E).

4. Effect of the conductive layer at Si-GaAs interface

4.1 Effect of carrier concentration at the GaAs–Si interface on the parasitic capacitance (simulation)

GaAs-on-Si wafers are expected to replace GaAs bulk wafers especially in GaAs power FET applications because they have high thermal conductivity, mechanical hardness in physical properties and advantages in material cost. But in microwave performances, MESFET's and HEMT's on Si have not always reached the same level of that on GaAs bulk wafers. This is mainly due to the parasitic capacitance originating from the conductive layer which is formed unintentionally during epitaxial growth of GaAs on Si by outdiffusion of Si atoms into GaAs. In this paragraph, the influence of the electron concentration in the conductive layer on the parasitic capacitance is studied using the ATLAS/BLAZE 2D heterostructure device simulator to simulate the gate pad capacitances[12].

Fig. 11 shows the simulated structure. The bottom of the wafer is a substrate of Si or GaAs. Layer (1) is the unintentional conductive layer which is assumed at worst to be 0.1 μm thick and to have n-type impurity of 1.0×10^{18} cm^{-3}. The symbols of G, S1, S2, and B stand for gate, source 1, source 2, and back-side electrodes, respectively. The calculated result of the pad capacitance as functions of the impurity (or free carrier) concentration and operating frequen-

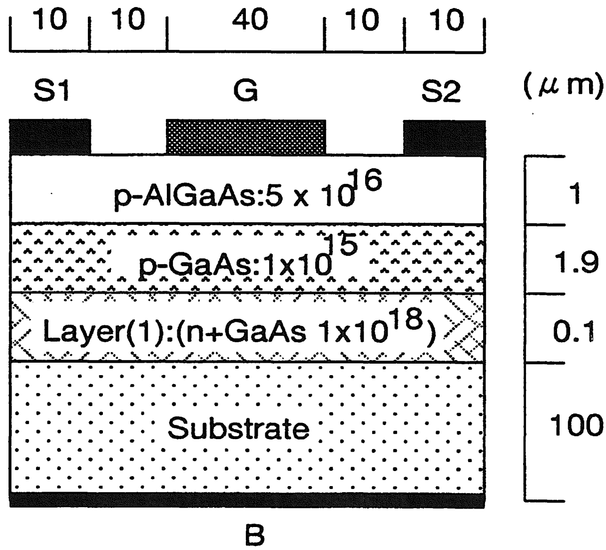

Fig. 11 The simulated structure. Layer (1) is the interface conductive layer.

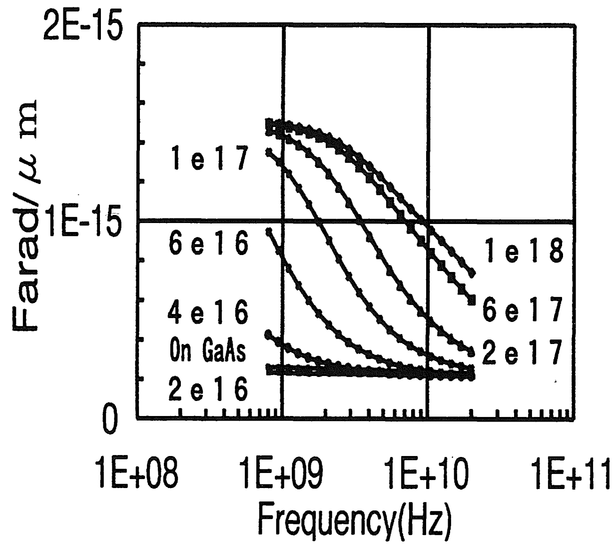

Fig. 12 Dependence of capacitance on the conductive layer impurity (or free electron) concentration.

cy is shown in Fig. 12, where the thickness of the conductive layer is fixed to 0.1 μm. It is found that even a carrier concentration of 4×10^{16} cm^{-3} makes the gate pad capacitance increase around the frequency of 1 GHz. As will be shown in the next paragraph, typical MOCVD

growth condition creates the interface free carrier whose density is about 2×10^{18} cm^{-3}. Therefore, the conductive layer due to the Si outdiffusion may arise serious effect on the high frequency performance of the GaAs-on-Si FET's.

4.2 Measurement of the interface carrier concentration by Raman scattering

The interface carrier concentration has been estimated using Raman scattering focusing on the coupled LO-phonon-plasmon mode (L+)[13]. The sample preparation procedure used in this experiment as shown in Fig. 13. A piece of the GaAs wafer was bonded onto a 600 μm thick GaAs bulk wafer using an epoxy resin. Then the Si substrate was completely removed by immersion in a 50% aqueous solution of KOH at about 90°C for 2–3 h. It was not possible to prevent the revealed GaAs thin plate from cracking. Therefore, several piece of GaAs thin platelets of several hundred micron squares which have (001) faces constitute the sample surface irradiated by a laser beam for the present Raman scattering measurement.

The Raman scattering experiment in which the sample is attached to a cryostat was performed at 80 K in a backscattering configuration to obtain well-resolved spectra by avoiding of the phonons due to lattice heating or hot-phonon effects. Raman spectra obtained from the GaAs back face of non-doped GaAs-on-Si's grown at the substrate temperatures of 750, 700 and 650°C are shown in Figs. 14(a), 14(b) and 14(c), respectively. It should be noted that the crystal quality at the back face is much lower than that at the usual front GaAs surface on Si due to the much more dislocations at the GaAs-Si interface through which Si atoms preferentially diffuse.

However, the phonon structures corresponding to the L+ mode in the measured Raman spectra in Figs. 14(a) and 14(b) are distinguishable enough for estimation of the carrier concentrations. In Fig. 14(c), no signals corresponding to the L+ mode are observed which indicates that the carrier concentration is below 5×10^{17} cm^{-3} since the present resolution limit has been found to be on this level in the calibration procedure using standard GaAs samples. In both Figs. 14(a) and 14(b) the L+ mode-related structures are quite broad and asymmetric, suggesting that the concentration in the measured region is inhomogeneous and has an abrupt distribution in depth. The spectrum structures of the Raman scattering are in the frequency ranges corresponding to the carrir concentrations from $1.2-4.5\times10^{18}$ cm^{-3} peaking at about 3.3×10^{18} cm^{-3} and in the range $0.9-2.7\times10^{18}$ cm^{-3} peaking at about 1.6×10^{18} cm^{-3} in Figs. 14(a) and 14(b), respectively. These values are fairly reasonable values as compared to those predicted previously[14].

It is concluded that there exists the conductive layers with the carrier concentration of 2×10^{18} cm^{-3} at the GaAs–Si interface for the growth temperature of 700°C which gives the best surface morphology for the present MOCVD system.

4.3 Effect of the conductive layer on the high frequency performance

A simplified equivalent circuit for the intrinsic region of a FET fabricated on a semi-insulating GaAs substrate is shown in Fig. 15(a), where Cgs, Ri, and g_D are a capacitance between the gate and the source, an input resistance, and a drain conductance, respectively. In the case of

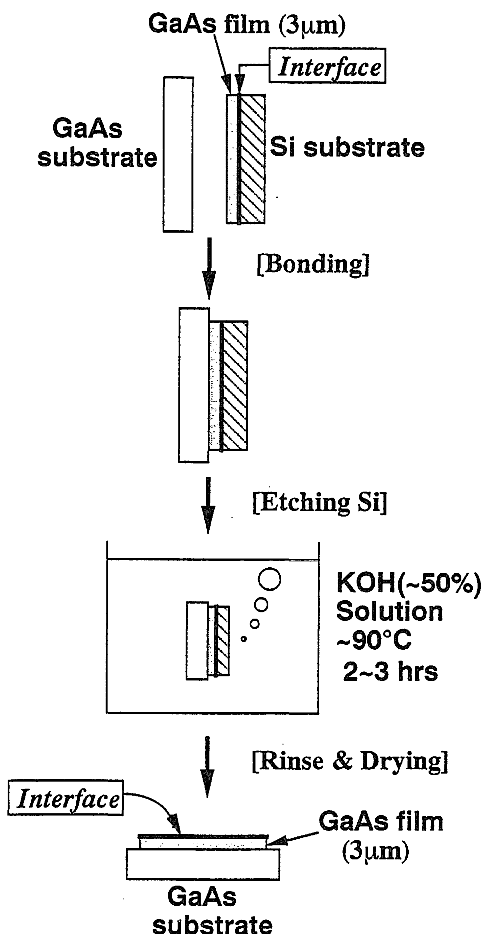

Fig. 13 Sample preparation procedure for Raman scattering measurement

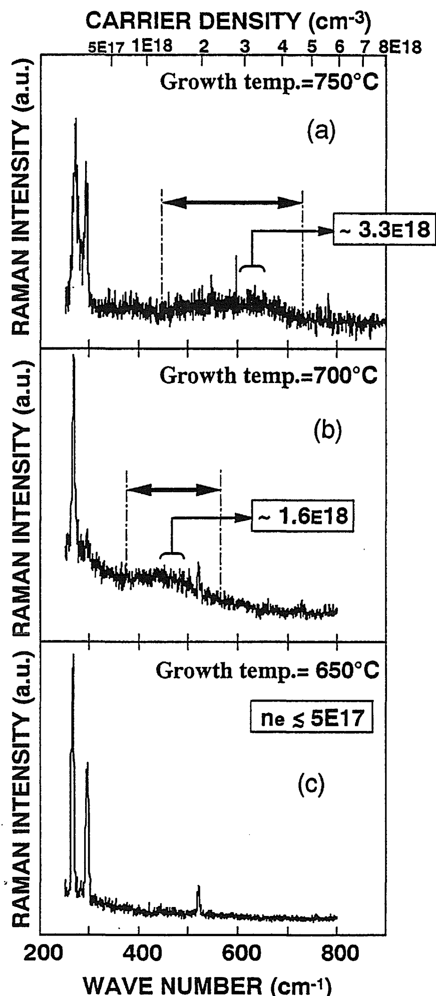

Fig. 14 Raman acattering spectra of the back faces of GaAs grown by MOCVD on Si at various temperatures: (a) 750°C (b) 700°C (c) 650°C.

GaAs-on-Si, the equivalent circuit may be represented by Fig. 15 (b) if the parasitic capacitance Cgp and resistance Rgp between the gate pad and the interface conductive layer is taken into account. The cut-off frequency f_T at which the current amplification factor h21 is equal to zero, is represented by

$$f_T \sim gm/2\pi Cgs(1+Cgp/Cgs) \tag{1}$$

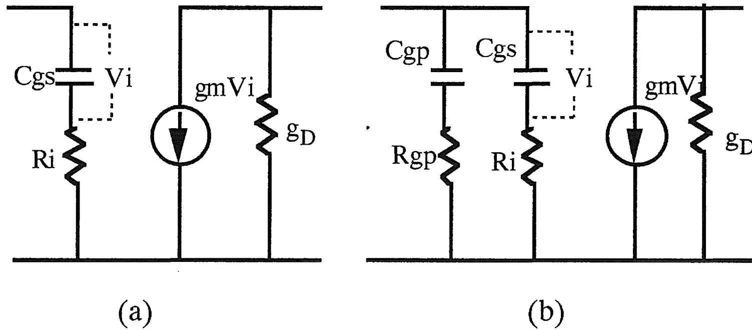

Fig. 15 Simplified equivalent circuit for (a) GaAs FET and (b) GaAs-on-Si FET.

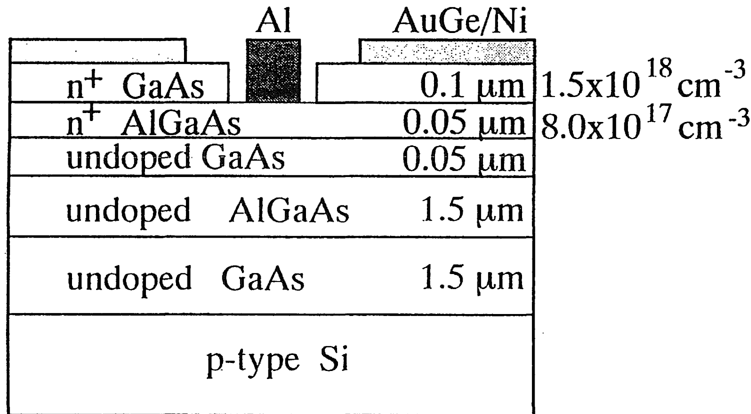

Fig. 16 Epi-layer structure for a fabricated HEMT.

in the case (b), whereas in the case (a) it is represented by

$$f_T \sim gm/2\pi Cgs.$$

Therefore, the point for the improvement in the high frequency performance is to reduce Cgp. To obtain the FET performance for GaAs-on-Si as good as for GaAs-on-GaAs, device structure which increases Rgp and/or decreases the ratio Cgp/Cgs is necessary provided that Cgp is inevitable in GaAs-on-Si.

A HEMT/Si as well as a HEMT/GaAs having the epi-layer structure as shown in Fig. 16 was fabricated for the purpose of studying the effect of the parasitic capacitance on the microwave performance. Here, the gate length and the width are 0.8 μm and 105 μm, respectively. The evaluation of the high frequency characteristics was made by measuring the S (scattering) parameters using a wafer probe in a frequency range of 1~20 GHz. Measured DC characteris-

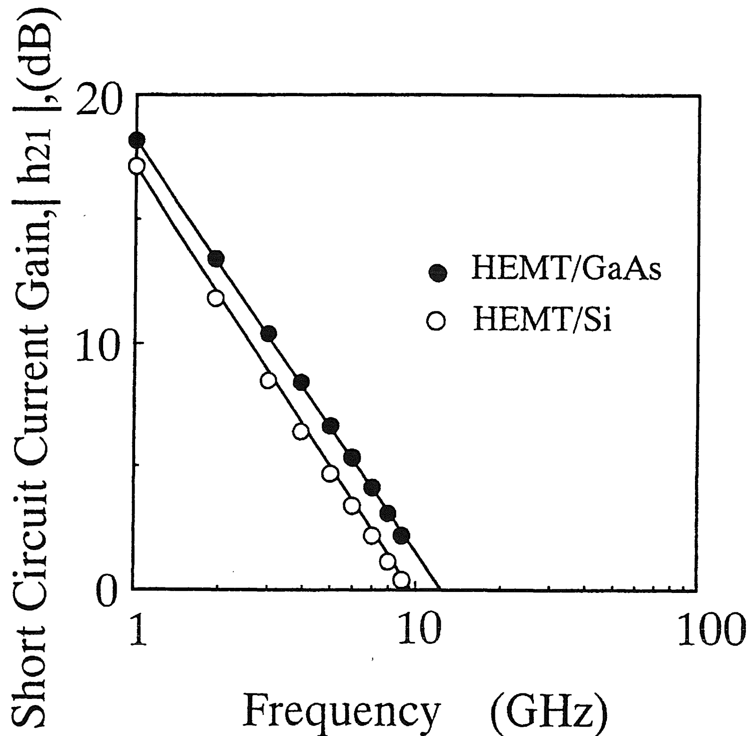

Fig. 17 Sort circuit current gain for HEMT/GaAs and HEMT/Si as a function of frequency.

tics for HEMT's on Si were almost the same as those on GaAs and both devices had a good gm value of 330 mS/mm. However, the cut-off frequency f_T measured for the device on Si was 9.8 GHz which is about 20% smaller than that on GaAs, that is, 12 GHz as shown in Fig. 17. Cgp's were determined to be 0.44 and 0.07 pF from the equivalent circuit analysis[15], which explain the decrease in f_T. The values of f_T and Cgp for HEMT's/Si were not dependent on the resistivity of the Si substrate. This fact indicates that the origin of the parasitic capacitance is not the conductivity of Si but the interface conductive layer.

4.4 Reduction of the parasitic capacitance

Methods for the reduction of the parasitic capacitance in GaAs FET devices on Si can be proposed as follows: (1) The area of the gate pad should be as small as possible (2) The distance between the pad and the conductive layer should be lengthened by inserting an insulating film like SiO_2, since Cgp is mostly occupied by the capacitance generated between the pad and the conductive layer.

Actually, when the pad area is reduced from 80 μm^2 to 50 μm^2, Cgp was reduced by half. In addition, insertion of 0.3 μm thick SiO_2 film gave another decrease in Cgp by half. Ex-

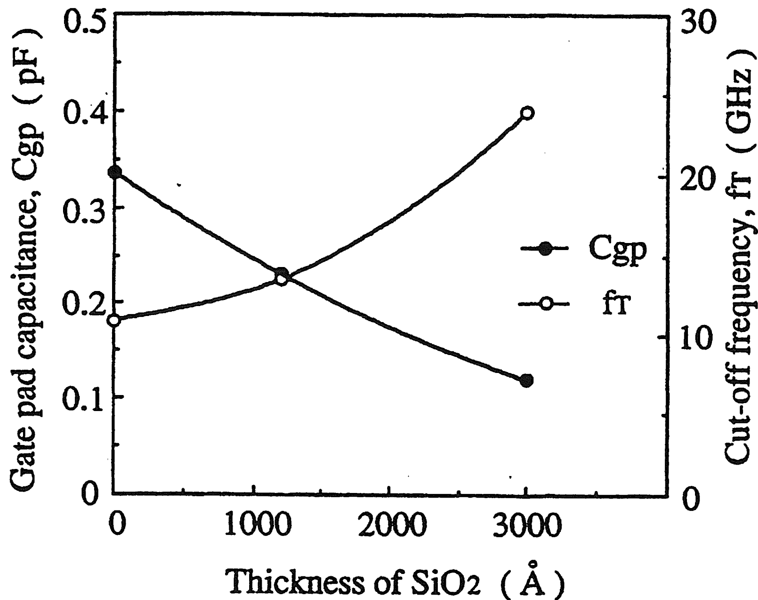

Fig. 18 Dependence of the gate pad capacitance Cgp and the cut-off frequency f_T on the thickness of SiO_2.

perimental result on the reduction of Cgp and f_T as a function of the inserted film thickness is shown in Fig. 18 which demonstrates that improvement of the high frequency performance can be attained by the proposed method.

5. Power GaAs FET on Si

It may be concluded on the basis of the discussion above that one of the most practical applications of GaAs-on-Si is power FET since power FET has quite large gate width and therefore large Cgs in the intrinsic region to control big current so that the ratio Cgp/Cgs in eq. (1) can be assumed small as compared to 1 and the effect of the parasitic capacitance may be negligible. In addition, advantage of GaAs-on-Si over GaAs bulk substrate in the thermal resistance is effectively given to the power MESFET which consumes high wattage and emits large amount of heat. Moreover, recently there is a great demand for high-output power and low-power consumption GaAs FET's for the mobile phones and their base-stations.

The structures of a fabricated MESFET/Si are illustrated in Fig. 19, which consist of a 0.2 μm thick GaAs buffer layer, a 1 μm thick AlGaAs buffer layer and a 0.3 μm thick GaAs active layer with a carrier concentration of 2×10^{17} cm^{-3}. Fabrication processes are carried out by mesa chemical etching for device isolation, AuGe/Ni ohmic contacts matallization and Al gate metallization after recess wet etching. After the gate metallization, a Si_3N_4 dielectric layer is attached for the surface passivation. Au plating is used for an air-bridge interconnection. As for

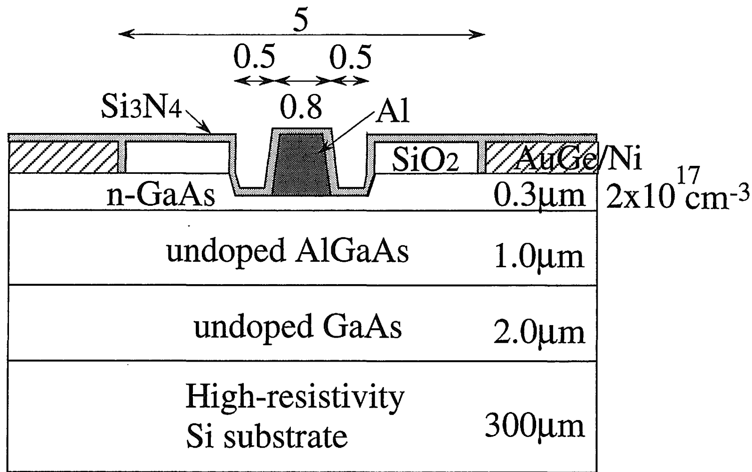

Fig. 19 Schematic cross-section for a fabricated MESFET/Si.

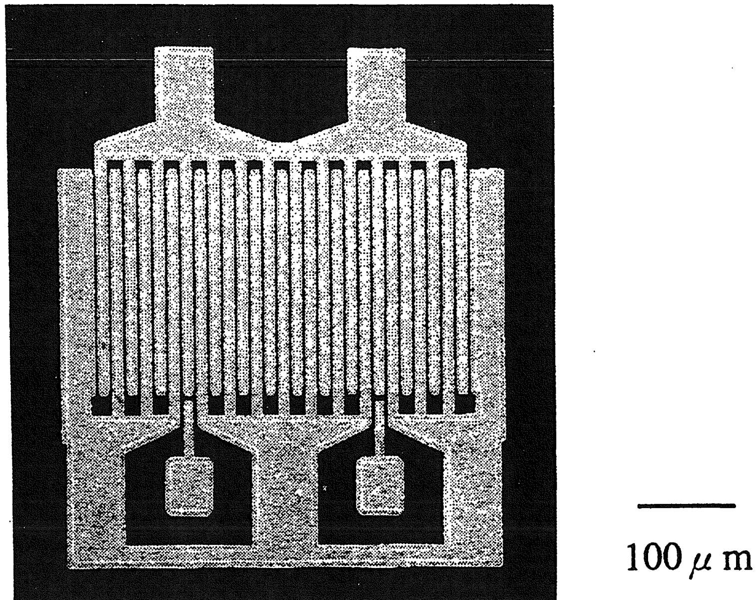

Fig. 20 A SEM photograph for a fabricated MESFET/Si.

the backside process of the wafer, Ti/Au multilayer is evaporated after thinning the Si substrate to 300 μm. A SEM photograph for the MESFET is shown in Fig. 20. A gate length and a width are 0.8 μm and 5.6 mm, respectively. The gate width is determined from desirable output power and a number of the gate pad is optimized for the width[16]. Each of the pad has an area of 50

μm^2, which is determined so as to let the total pad capacitance be less than 10% of Cgs for the MESFET[8]. As for the pad capacitance and Cgs used in the determination, the former is based on the HEMT/Si evaluation and the latter is calculated at the condition of zero gate bias. A gate bus-line, which connects each of gate fingers, can increase another parasitic capacitance considered as Cgp if it is formed directly on a buffer layer of the wafer. Therefore, a SiO_2 dielectric layer with a thickness of 0.3 μm is inserted under the gate bus-line[8].

The typical current-voltage characteristics for a fabricated MESFET/Si indicate that a source-drain saturation current is ~180 mA/mm and the maximum transconductance is ~120 mS/mm. A gate-drain breakdown voltage of $-12\sim-14$ V is obtained as measured at a gate reverse current of 500 $\mu A/mm$. These dc characteristics are almost the same as those for a MESFET/GaAs fabricated simultaneously. S-parameters are measured to evaluate the parasitic parameters for the MESFET/Si at Vds of 2.0 V and Vgs of showing the maximum transconductance. From the extraction of equivalent circuit parameters, it is pointed out that the ratio of Cgp including the gate bus-line to Cgs can be reduced to ~10%, which is almost comparable to that of 5~7% for the MESFET/GaAs. The result indicates that the reduction for a ratio of Cgp/Cgs is actually achievable for a large gate width device by considering a size for the gate pad and a structure for the gate bus-line.

An input-output characteristic for the power MESFET/Si is shown in Fig. 21. The MESFET is mounted in a package and measured at a frequency of 0.85 GHz, a source-drain voltage of 3.6 V and a source-drain current of ~10% of Idss. The measurement condition means the ap-

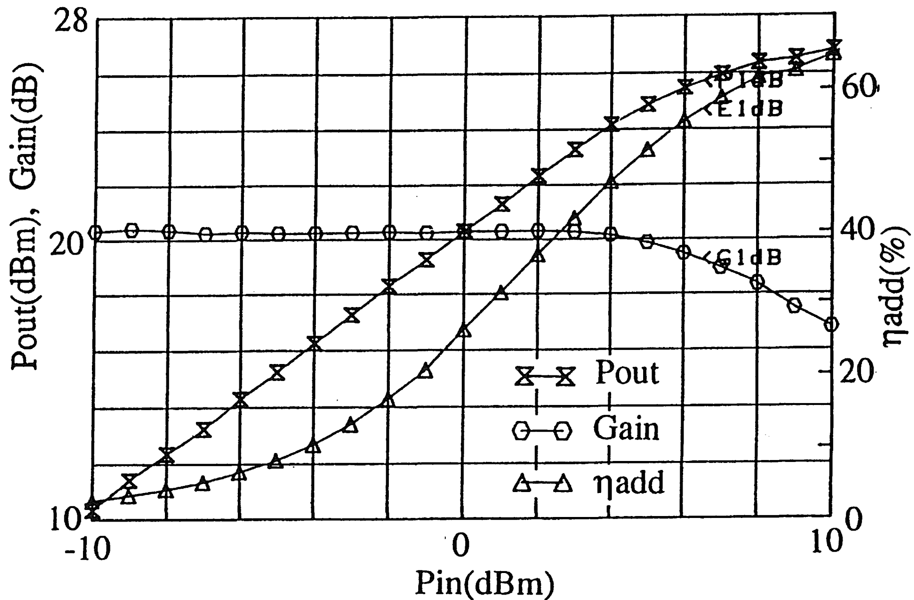

Fig. 21 Input-output characteristic for a fabricated power MESFET/Si (gate length Lg=0.8 μm, gate width Wg=5.6 mm).

plication of the MESFET to a mobile communication system such as a handy phone. After taking impedance matching for input and output using S-parameters, an optimum load impedance is determined by a load-pull and a source-pull method so as to obtain maximum output for an input power of 10 dBm. As can be seen in Fig. 21, the MESFET demonstrates output power at 1 dB compression ($P_{1\,dB}$) of 25.7 dBm, linear gain (G_L) of 20.5 dB and power added efficiency (η_{add}) at 1 dB compression of 57%, which are comparable to those for a MESFET/GaAs commercially fabricated. The same evaluation as indicated in Fig. 21 is carried out in the case of a lower source-drain voltage and shown in Fig. 22. It is found in Fig. 22 that G_L and η_{add} can be hardly degraded even at a source-drain voltage as low as 2.4 V.

In summary, The parasitic capacitances and resistances peculiar to GaAs/Si electronic devices caused by a Si-GaAs interfacial conductive layer have been evaluated. From the evaluation, a large gate width device is expected to be the most suitable application for the GaAs/Si because such a device can reduce a ratio on an extra input capacitance for the gate pads, which is a major cause to degrade microwave performance, to an intrinsic input capacitance. A fabricated power MESFET/Si with a relatively small area for a gate pad and a gate bus-line under which a dielectric layer is inserted can actually reduce the ratio in eq. (1) as comparable as to that for a MESFET/GaAs. The MESFET/Si demonstrates the parameter values of P_{1dB}, G_L and η_{add} as high as those for MESFET/GaAs. Moreover, almost the same values are obtained even at a source-drain voltage of 2.4 V. The result indicates that the GaAs/Si is adequately substitutable for GaAs/GaAs in the application for mobile communication devices driven by a low supply voltage.

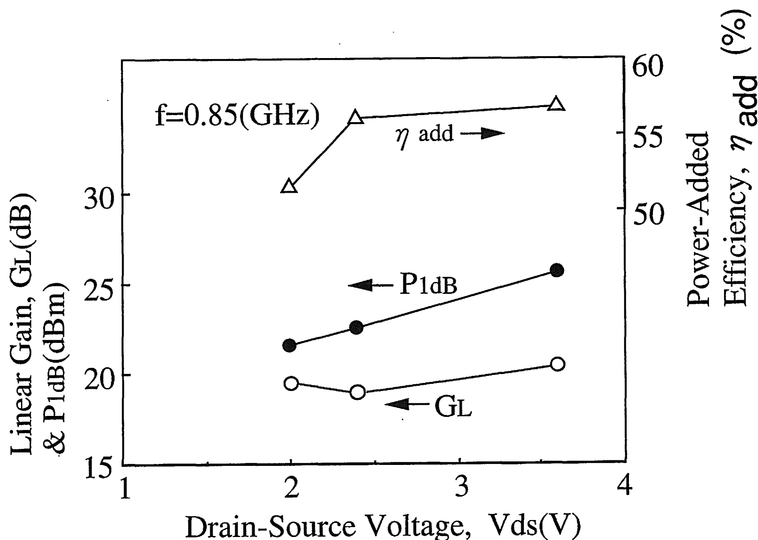

Fig. 22 Dependence of linear gain (G_L), output power (P_{1dB}) and power-added efficiency (η_{add}) on drain-source voltage (Vds).

6. Summary and Prospects

Various electronic devices with the use of GaAs-on-Si wafers have been fabricated from 1984 to date, but failed in the practical use. The reason why they have not yet reached the practical use is clarified in this paper by fabrication of MESFET's and HEMT's on Si.

Firstly, it is pointed out that the failure in the application to integrated circuits for practical use which requires reliability of the devices is partly due to the interaction between the dislocations and implanted species as shown in sec. 3.2, on the one hand. On the other hand, all epitaxially grown and fabricated HEMT and MESFET on Si are not related to the dislocations and excellent uniformity in Vth is obtained in these devices.

Secondly, the inferior performance for high frequency in the GaAs-on-Si to that in GaAs-on-GaAs is found to be due to the free carriers at the interface conductive layer which creates the parasitic capacitances. This fact has also prevented the practical use of the devices. However, the ideas for the reduction of the parasitic capacitances in the fabrication process in this work has successfully overcome this difficulty. Furthermore, it is also pointed out that in the power MESFET with large gate area the ratio of the parasitic capacitance to the intrinsic capacitance is negligibly small so that almost the same high frequency performance in the GaAs-on-Si can be obtained as in the GaAs on GaAs.

Once these problems considered to be inherent to GaAs-on-Si are resolved, the advantage of GaAs-on-Si over GaAs-on-GaAs, that is, low thermal resistance, low cost, large diameter wafer, ecologically safe and so on becomes attractive in the practical use. Actually, the GaAs-on-Si wafers grown by the present author and co-workers have been utilized in the fabrication of power MESFET's for mobile phones and their base-stations by one of the major electronic device makers and now these devices are under reliability test in the factory.

Therefore, it is expected that in the very near future the power MESFET will be the first runner for the practical use of GaAs-on-Si.

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