*Shimane Ika Daigaku Kiyo (Bull. Shimane Med. Univ.)*
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# An Inexpensive Pulse Programmer for Transient NQR Experiments

(NQR/instrument)

Mitsuo MISHIMA *

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A four-channel pulse generator has been constructed using inexpensive digital integrated circuits. At a total component cost of ¥ 80,000, the device can program the pulse width, the delay time, and the trigger period within an accuracy of 1 ppm. The preset time can be adjusted in the range from 0.5 $\mu$s to 9990 s. A sequence of pulses can be repeated up to 999 times. The whole circuit and its timing chart are represented in detail.

## INTRODUCTION

The spin echo and the free induction decay experiments in NQR have been developed mainly by Hahn *et al.* [1] These techniques have been used to investigate the relaxation processes. Some interesting results have so far been obtained.[2,3] Many reports on the instruments for the transient experiments have also been published.[4-8]

The rf pulses can be generated by switching an rf oscillator or a power amplifier. Then, the widths of the on-off pulse and the pulse intervals must be reproduced within an accuracy of 1 ppm. Furthermore, the pulse generator meets the requirement that the wide-ranging time data, usually from 1 $\mu$s to 1000 s, should be set up with ease. Unfortunately, most commercially available instruments are exceedingly costly owing to their complex design. It was decided, therefore, to investigate a new simplified design based on the use of integrated logic circuits. The 74LS-type of the TTL circuits which are now supplied at a low cost have the rise time of 8 ns and the propagation time of 9 ns. This sufficiently satisfies the switching characteristic of the pulse programmer.

In the constructed circuit, the pulse width, the pulse interval, and the iteration period can be set up in the range of 0.5 $\mu$s to ca. $10^4$ s. The pulse sequence which consists of 4 pulses maximally can be iterated up to 999 times. This instrument can also be applied to the ultrasonic echo and the pulsed NMR. In most cases, the high-voltage pulses are fed to the grid gate of the vacuum tube. This can easily be made possible by use of a high-speed power MOSFET.

* *Department of Chemistry*

## DESIGN

The block diagram of the pulse programmer is shown in Fig. 1. The data on the pulse width ($t_w$), the pulse interval ($\tau$), the iteration period (T), and the iteration number (N) are stored in the memories I and II. However, the data on $t_w$ are read out from the memory I alone. The data on $t_w$ and $\tau$ are memorized in the addresses from 0 to 7, whereas those on T and N are written in the addresses of 8 and 9, respectively. The datum on the time is inputted in the form of $x\times10^y$, where $x$ is a positive number of three figures and $y$ is a number from $-6$ to 1. The value of N is given by $x$ alone. A sequence of control pulses which the timing controller generates are used for reading out the data in the addresses of 8 and 9 and for loading to the T-counter and the N-counter. The last of the timing pulses opens the clock gates which are connected to the master counters A and B. Simultaneously the address of the memory I is set 0, and the datum is loaded to the comparator I, whereas the address number of the memory II is always kept smaller than the memory I by 1. On the other hand, the flip-flop circuit of the pulse generator (see Fig. 8) is cleared.

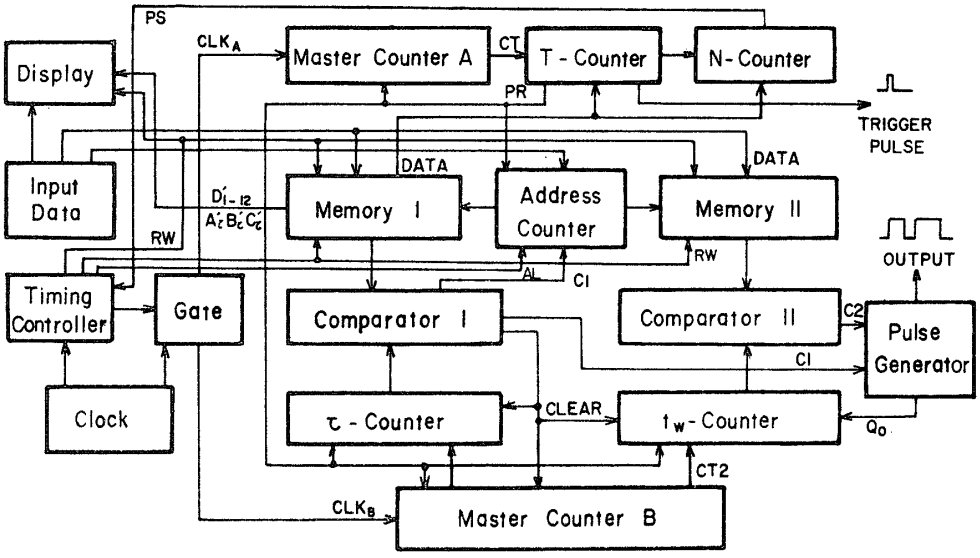



Fig. 1. Block diagram of pulse programmer.

The gate of the $t_w$-counter is closed when the output of the flip-flop circuit is low. At the same time that the datum in the $\tau$-counter comes up to that in the memory I, the output of the flip-flop goes towards to the high level. Then, the addresses of the two memories are set 2 up, and the corresponding data are transferred to the comparators. At this time, the $\tau$-counter and the $t_w$-counter count up the clock signals. Though the coincidence pulse of the comparator II makes the output of the flip-flop low, it does not contribute to changes of the address numbers of the memories. The $\tau$-counter operates until it counts the clock pulses up to the setup number. The coincidence pulse from the comparator I clears the master counter B, the $\tau$-

counter, and the $t_w$-counter. This pulse increases the address numbers of the memories I and II by 2 through the address counter. This step cycle is repeated until the fixed time set by the T-counter. The reset pulse of the T-counter clears all the counter, gives the clock pulse to the N-counter, triggers a synchroscope and/or a boxar integrator, and loads the datum in the register to the T-counter itself again. The device repeats the same action from the first until the N-counter commands to stop.

*I. Data Input Circuit*

The negative logic datum is fed to the input terminals of the circuit shown in Fig. 2 through the so-called diode matrix. The datum is led to the desired register unit by turning on one of the switches ($SW_{1-3}$). $SW_1$ is used to designate the input data as the address number. On turning on $SW_2$, the datum is led to the shift register (74LS195). This is assigned to the integer part of the time datum. The exponent part of the datum is stored in the parallel register (74LS175) by turning on $SW_3$, and is converted to a number ranging from 0 to 7 by the circuit composed of the AND and OR gates. $SW_4$ is used to change the sign of the exponent part. The data except the address number can be cleared by $SW_5$.

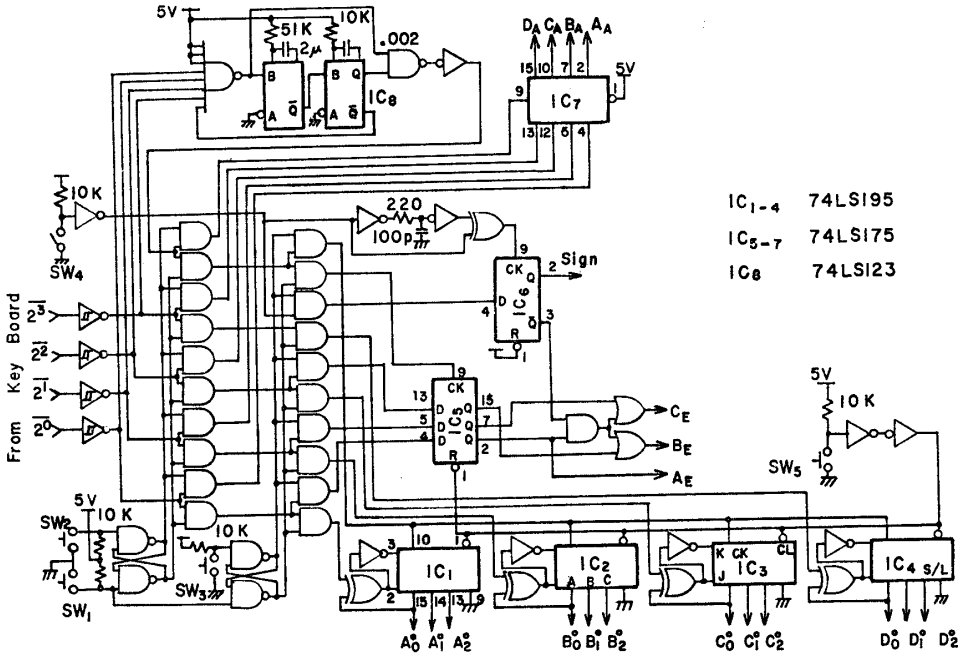



Fig. 2. Data input unit.

*II. Timing Controller*

Figure 3 shows the circuit of the timing controller. The data in the registers can be written in the memories by turning on $SW_9$. A sequence of timing pulses are generated by turning on $SW_8$. Some important charts of these pulses are shown in Fig. 4. (TNL) and (TNA) are used for loading the datum from the memory I to the T-counter unit and for latching the

register, respectively. (TNL) is also used to load the datum on N to the N-counter. On the other hand, (AL) loads the datum set up by the timing controller to the address counter. (TLO) opens the clock gates. The standard clock pulse generator is shown in Fig. 5. $SW_{10}$ selects either the 1 MHz clock or the 2 MHz clock. The desired stability of the clock was easily attained by use of the crystal oscillator (Asahi Denpa Co., MA110A).

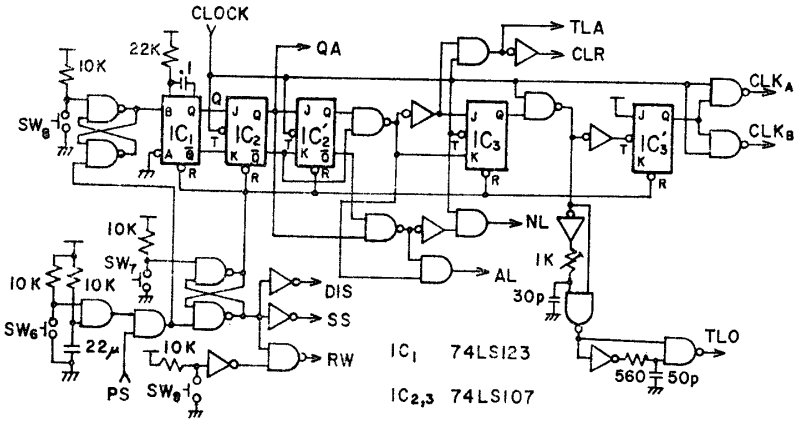



Fig. 3. Timing controller.

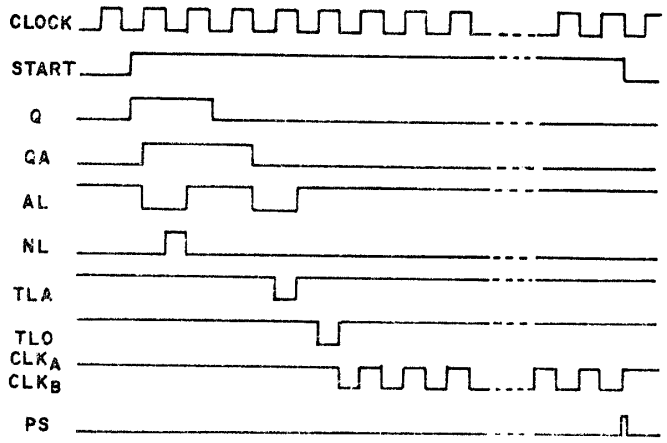



Fig. 4. Timing charts.

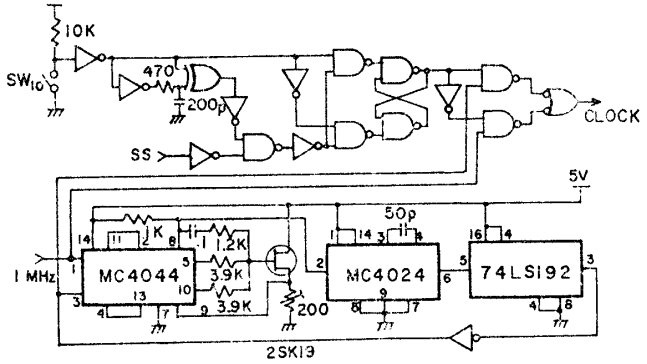



Fig. 5. Clock pulse generator.

## *III. Master Counters*

The clock pulses from the NAND gate of the timing controller are devided by the master counter composed of 7 synchroneous decade counters, as shown in Fig. 6. The master counter B provides the clock signals to both the $\tau$-counter and the $t_w$-counter. In the case of the master counter A, one of the multiplexers comes into disuse. ($A_T$, $B_T$, and $C_T$) are fed to the input terminals of the multiplexer instead of ($A_\tau$, $B_\tau$, and $C_\tau$) or ($A_t$, $B_t$, and $C_t$). The output clock signal is designated as (CT). The output of the multiplexer is fed to the OR gate along with the clock pulse. This is in order to recover the propagation delay caused by the multiplexer and the buffer gates.

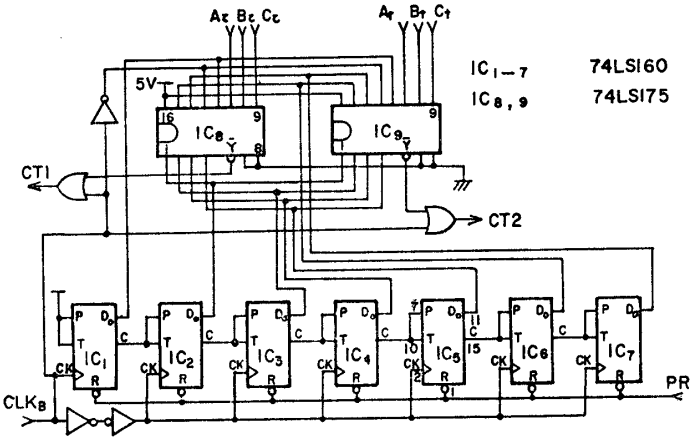



Fig. 6. Master counter B.

## *IV. T-Counter and N-Counter*

Figure 7 shows the circuits of the T-counter and the N-counter. The T-counter is composed of the D-latch registers, the decade up-down counters, and the gate circuits. One of the registers stores the information on the exponent part of the datum that controls the multiplexer of the master

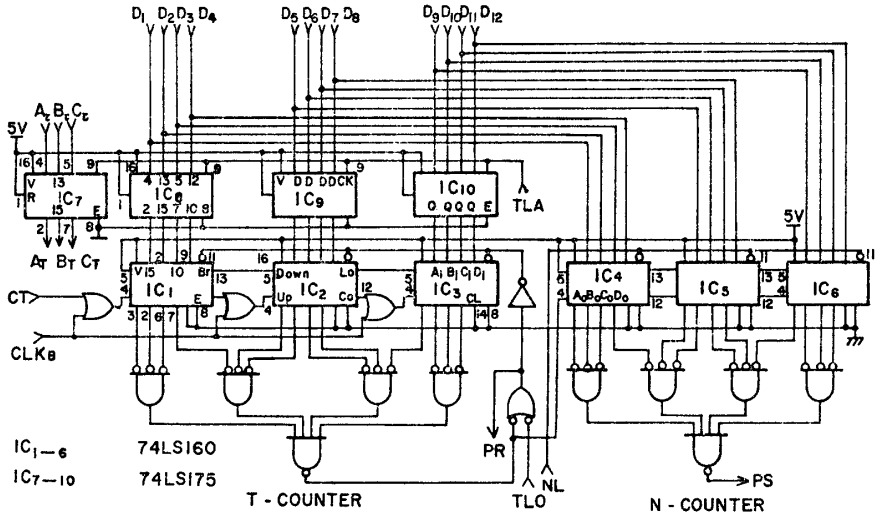



Fig. 7. T-counter and N-counter.

counter A. The clock pulse from the master counter counts down the preset number. The borrow-in signals of the decade counters are synchronized by the OR gates inserted between the counter IC's. The coincidence pulse from the four-input NAND gate functions as the borrow-in signal for the N-counter, and loads the datum to the T-counter. (PR) clears all the counters. (PS) closes the clock gate of the timing controller.

## *V. $\tau$-Counter and $t_w$-Counter*

The $\tau$-counter unit consists of the memory, the comparator, and the $\tau$-counter, as shown in Fig. 8. Three of the memory IC's store the integer part of the datum, and the other stores the decoded exponent part. The integer part of the datum is transferred to the comparator through the demultiplexer composed of the NOR gates, whereas the exponent part is led to the master counter B. The coincidence pulse of the comparator (C1) leads the master counter B, the $\tau$-counter, and the $t_w$-counter. (C1) is also transferred to the address counter and the pulse generator. The $t_w$-counter unit has fundamentally the same construction as the $\tau$-counter one. In the $t_w$-counter unit the demultiplexer is replaced with the inverters. The (# 1) terminal is controlled of the pulse generator, though in the $\tau$-counter unit it is connected to the power supply line. When (Q) is low, the functions of the $t_w$-counter unit are at a stop.

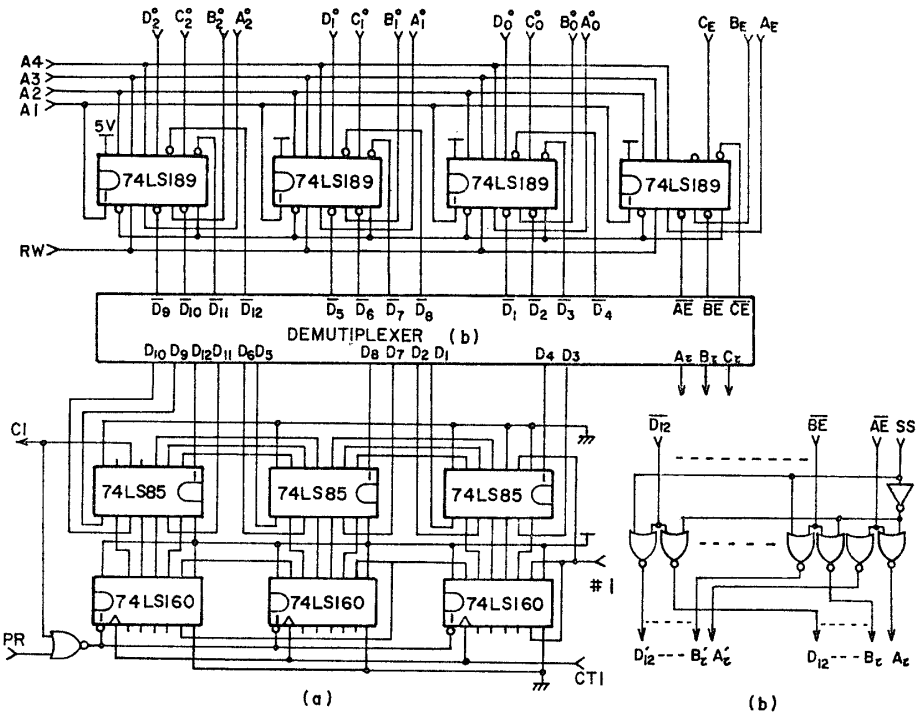



Fig. 8. $\tau$-counter unit.

## *VI. Address Counter and Pulse Generator*

Figure 9 shows the circuit of the pulse generator and the address counter. (C1) serves as a clock signal for the address counter. The output terminal of

the most significant figure of the binary counter is utilized as that of the least significant figure. Therefore, the datum accumulated in the counter is set 2 up by (C1). According to (SS), the multiplexer selects either the datum in the counter or that in the register. When (SS) is high, the address number of the data input circuit is fed the $\tau$-counter and the $t_w$-counter. Then, both of the counters have the same address number. In this state, to write in the memories and load to the display unit is possible. When (SS) is low, the datum made up by the address counter is selected as the address number. In this case, the number which is smaller by 1 than the datum in the address counter is loaded to the $t_w$-counter. This subtraction is carried out by the full adder (74LS83).

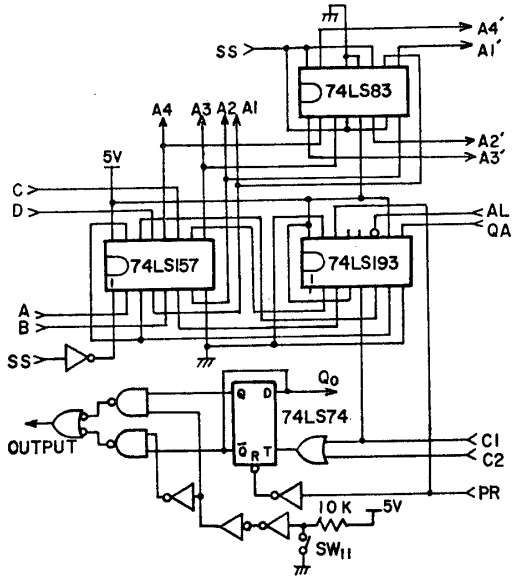
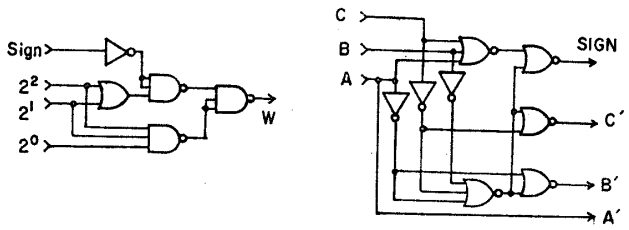



Fig. 9. Address counter and pulse generator.

The action of the pulse generator is very simple. First, the output of the edge-trigger D-flip-flop is forced to be low by (PR). Second, (C1) makes the output of the flip-flop high. Next, this output is lowered when (C2) turns up. After that, this action is repeated until the clock gates are closed. Either the positive or the negative pulse sequence is selected by controlling the panel switch ($SW_1$).

*VII. Display Circuit*

The display circuit was constructed of the 7-segment LED's and the LED drivers. This circuit is well-known. The accessories of the display circuit are shown in Fig. 10. The circuit (a) is used to send out a warning when a forbidden number is set on as the exponent part of the datum. If this is the case, (W) becomes high. The decoded exponent part of the datum stored in the memory I is returned to the former state by the circuit (b).




(a) (b)

Fig. 10. Accessories of display circuit. (a) Warning circuit and (b) encoder of exponent part of time datum.

## OPERATING SPECIFICATIONS

(1) Range of preset time: 0.5 $\mu$s—9990 s
(2) Maximum pulse number: 4.
(3) Maximum iteration number of pulse sequence: 999.
(4) Characteristic of output pulse:

| | |
|---|---|
| Pulse hight | ca. 4 V |
| Rise time | 12 ns |
| Fall time | 12 ns. |

(5) Clock stability: within 1 ppm.
(6) Error of pulse width: 10 ns.
(7) Power supply: 5 V with 1.6 A.

This pulse programmer responded even to the 7.5 MHz clock. The period of time that elapses between the moment (C1) rises and the moment the next datum is loaded to the comparator again is 70 ns. It is, therefore, expected that an insignificant improvement makes this circuit respond to the 10 MHz clock. If the crystal oscillator is thermostated with $\pm 0.1°$, the stability of the clock will be increased up to 0.1 ppm.

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