Hot-Carrier-Degradation of Hetero-Interface in SiGe/Si-Hetero-MOSFETs

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Strained-Si and SiGe/Si hetero-CMOS structures are highly promising materials for the construction of advanced high performance Si CMOS devices [1]. To exploit the advantages of the SiGe/Si heterostructure effectively and to establish adequate device reliability, an understanding of the electrical properties of the hetero-interface, i.e., hetero-interface traps, is important.

In this paper, it is shown that hetero-interface traps are generated by hot carrier stress in the SiGe/Si heterostructure, and the trap density is roughly estimated.

SiGe-channel pMOSFETs, as shown in Fig. 1, were used in this study. A Ge fraction of 0.4 was used, and the gate length L and width W were 1 μm and 4 μm, respectively. These devices were fabricated using a low-temperature, high-quality, strained epitaxial heterostructure growth technique based on ultra-clean low-pressure CVD [2]. The hot carrier stress was applied at a drain voltage V_D of -8 V and a gate voltageV_G of -1 V or -2 V for 10 min. Charge pumping (CP) measurements [3] were performed using a gate pulse of fixed amplitude (-3 V) and a variable base level V_{BASE}, with a pulse frequency f of 250 kHz.

We recently introduced a new technique based on CP to measure the SiGe/Si hetero-interface trap density N_{it} in a SiGe pMOSFET [4]. The CP characteristics of a SiGe pMOSFET at RT and low temperatures are shown in Fig. 2. With decreasing temperature, the CP characteristics exhibit a clear plateau in the region of V_{BASE}>2.4 V. The CP current I_{CP} in the plateau region is only due to the hetero-interface traps, and I_{CP} from the gate oxide interface-traps is suppressed in this region. Therefore, N_{it} can be derived from the following equation; $I_{CP}=f \cdot q \cdot L \cdot W \cdot N_{it}$. The value of N_{it} before hot carrier stress obtained from Fig. 2 is 5×10^{10} cm^{-2}.

The CP characteristics before and after hot carrier stress in the SiGe pMOSFET are shown in Figs. 3(a) at RT and (b) at 91 K. With decreasing temperature, I_{CP} in the notable region of V_{BASE}>2.4 V decreases significantly, and its form also changes. We confirmed that the ration of substrate current to drain current I_{SUB}/I_D and gate current I_G in a SiGe pMOSFET decreased during stressing, and the linear maximum transconductance increased after stress, which suggests that negative charge is generated in the gate oxide near the drain due to trapped electrons, and V_T is increased near the drain due to the negative charge [5]. As will be explained later, the increase in I_{CP} in the region of V_{BASE}>2.4 V in Fig. 3(e) at 91 K is due to SiGe/Si hetero-interface traps generated by hot carriers. The density of the generated traps is estimated to be $1\text{-}3\times10^{12}$ cm^{-2}, assuming that the effective lateral width of the hot-carrier damaged region is 0.1-0.2 μm.

The CP characteristics after hot carrier stress measured under two different conditions are shown in Figs. 4(a) and (e), i.e., with both the source and drain connected, and with the drain disconnected. A schematic representation of the inversion layer formed at the lower level V_L of the gate pulse during CP measurements in the indicated specific V_{BASE} region is shown in 4(b)-(d) at RT, and in 4(f)-(h) at 91 K. The higher V_T region near the drain is due to trapped electrons. For V_{BASE}>3.5 V at RT and V_{BASE}>3.3 V at 91 K, and with the drain disconnected (Figs. 4(b) and (f)), I_{CP} is not observed, as shown in Figs. 4(a) and (e), because an inversion layer can not be formed both in the SiGe layer and the surface Si layer at V_L. When the source and drain are connected (Figs. 4(c) and (g)), an inversion layer can be formed in the higher V_T region near the drain, because carriers are supplied from the drain side at V_L. In these cases, I_{CP} is observed as shown in Figs. 4(a) and (e). However, an inversion layer can not be formed in the surface Si layer at 91 K, and thus the measured I_{CP} in the V_{BASE} region should be due in part to hot-carrier-generated hetero-interface traps, as shown in Fig. 4(g). Moreover, with decreasing V_{BASE} with the drain disconnected, an inversion layer begins to form, because carriers are supplied from the source side at V_L (Figs. 4(d) and (h)). In these cases, an inversion layer can also be formed in the higher V_T region, because carriers flow into the region from the source side. However, an inversion layer can not be formed in the surface Si layer at 91 K, and therefore the measured I_{CP} in the region between 2.4 V< V_{BASE}<3.3 V should be due to hetero-interface traps in the entire SiGe/Si heterostructure including the hetero-interface traps generated by hot carriers, as shown in Fig. 4(h).

Therefore, we can obtain the hot-carrier-induced hetero-interface trap density from the CP current in the higher V_{BASE} region at a sufficiently low temperature.

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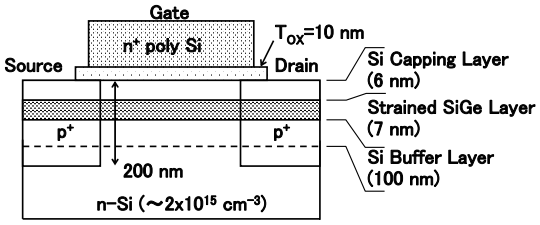

Fig. 1 Schematic cross section of SiGe-pMOSFETs

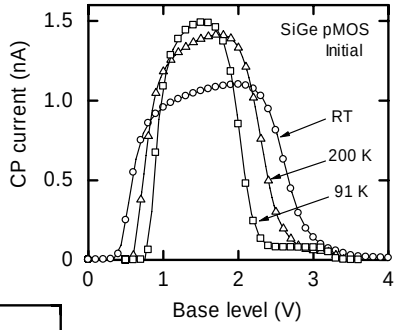

Fig. 2 Charge pumping characteristics before stress at RT and low temperatures.

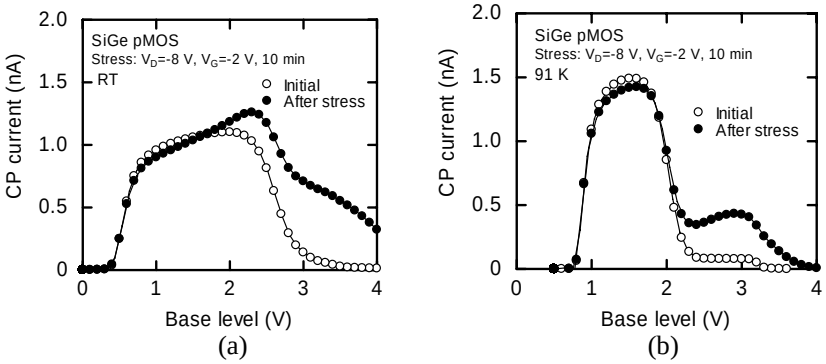

Fig. 3 Charge pumping characteristics before and after stress (a) at RT, and (b) at 91 K.

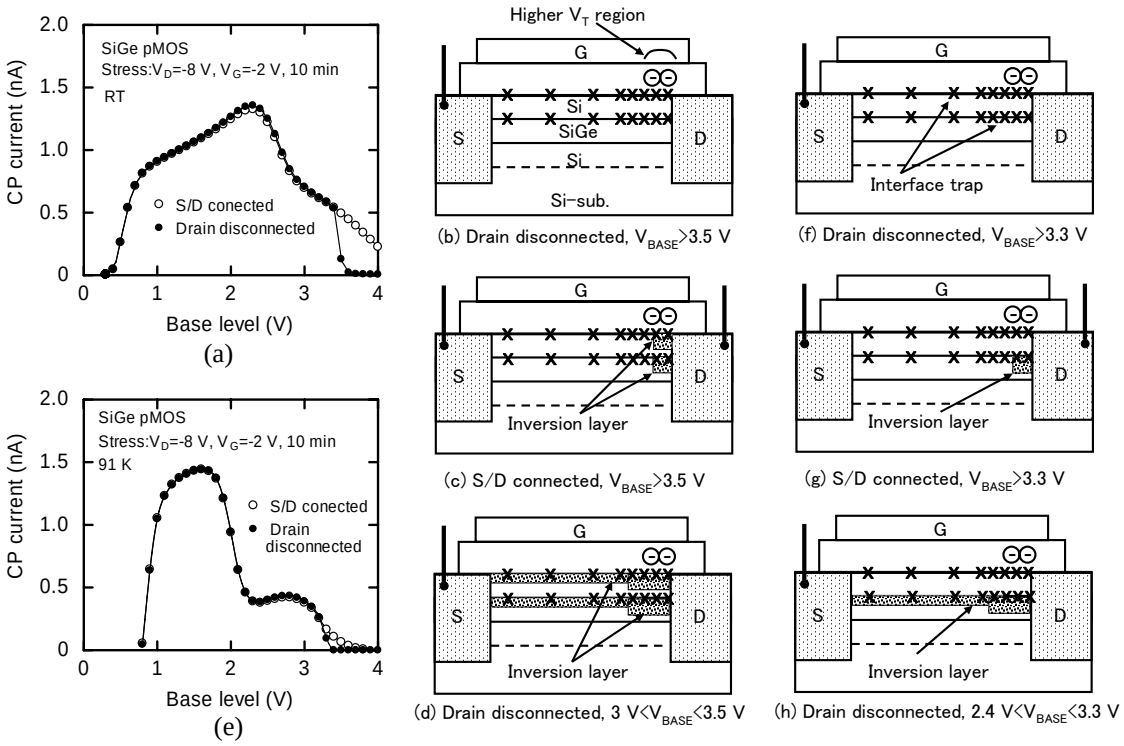

Fig. 4 Charge pumping characteristics measured under two different conditions, i.e., both source and drain terminals connected, and with the drain terminal disconnected, in a hot-carrier-stressed SiGe pMOSFET (a) at RT, and (e) at 91 K. Schematic representation of the inversion layer formed at the lower level of the gate pulse during charge pumping measurements in the indicated specific base level of the pulse, (b)-(d) at RT, and (f)-(h) at 91 K.