Characterization of Hot-Carrier Degraded SiGe/Si-Hetero-PMOSFETs

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Abstract

Hot-carrier degraded SiGe/Si-hetero-pMOSFETs have been characterized. The degradation of transconductance and the threshold voltage shift after hot-carrier stress are discussed based upon the changes in the densities of SiGe/Si hetero-interface traps and gate-oxide interface traps, which have been evaluated using a unique low-temperature charge-pumping method. It is concluded that the increase in the maximum transconductance and the threshold-voltage shift after a hot carrier stress are mainly due to trapped electrons in the gate oxide near the drain, and the decrease in transconductance, dependent on the gate voltage, is considered to be due to generated SiGe/Si hetero-interface traps.

Keywords: Metal-oxide semiconductor (MOS) devices, Silicon Germanium, Hot carrier effects, Interfaces

1. Introduction

Strained-Si and SiGe/Si hetero-CMOS structures are highly promising materials for the construction of advanced high-performance Si CMOS devices [1][2]. However, there are few reports on the reliability issues that affect these devices.

Hot-carrier degradation in the device characteristics of conventional Si-pMOSFETs is mainly caused by trapped-electrons in the gate oxide and/or hot-carrier-induced interface traps between the gate oxide and the silicon surface. Recently, it has been found that SiGe/Si hetero-interface traps are induced by hot carriers [3].

In this paper, we describe and discuss the characteristics of hot-carrier-degraded SiGe/Si-hetero-pMOSFETs.

2. Experimental

The devices used in this study were strained-SiGe-channel pMOSFETs, fabricated using low-temperature, high-quality, epitaxial heterostructure growth by ultraclean low-pressure chemical vapor deposition, comprising a 100-nm thick Si-buffer layer, a 7-nm thick strained-SiGe layer, and a 6-nm thick capping Si layer [4]. The Ge fraction in the SiGe layer was 0.4, and the gate length and width were 1 μm and 4 μm, respectively. All of the annealing processes were performed at temperatures below 700 C to prevent degradation of the heterostructure surface flatness and change in the Ge depth-profile in the channel region. Hot-carrier stress was applied at a drain voltage (V_D) of -8 V and a variable gate voltage (V_G) for 10 min. Threshold-voltage

shift, transconductance (g_m) degradation, and changes in charge pumping current after hot-carrier stress were all evaluated. Charge pumping measurements were performed using a gate pulse of a fixed amplitude (-3 V) and a variable base level (V_{BASE}), at a pulse frequency of 250 kHz.

3. Results and discussion

Typical drain-current and g_m dependences upon V_G before and after hot-carrier stress are shown in Fig. 1. The figure indicates the increases in the maximum g_m and the threshold voltage (V_T) after the stress. We also confirmed that substrate current (I_{SUB}), due to impact ionization during the stress, decreases, indicating negative charge generation due to electrons trapped in the gate oxide near the drain [3][5]. The degradation rate of the maximum g_m and the V_T shift dependencies upon stress V_G are shown in Fig. 2. I_{SUB} and a gate current (I_G) at V_D of -8 V are also shown in the figure. I_G is due to electrons which have been injected into the gate oxide and reach the gate electrode. From the figure, it is found that the device degradation rate corresponds well with the behavior of I_G, but not with that of I_{SUB}. Therefore, it can be concluded that the increases in the maximum g_m and V_T after the stress were caused mainly by trapped electrons in the gate oxide near the drain.

However, a decrease in g_m can be seen after the stress in the V_G range from -0.3 to -1 V as shown in Fig. 1. This behavior can not be explained by the trapped electrons in the gate oxide. It may be caused by hot-carrier-induced gate-oxide interface traps and/or SiGe/Si hetero-interface traps.

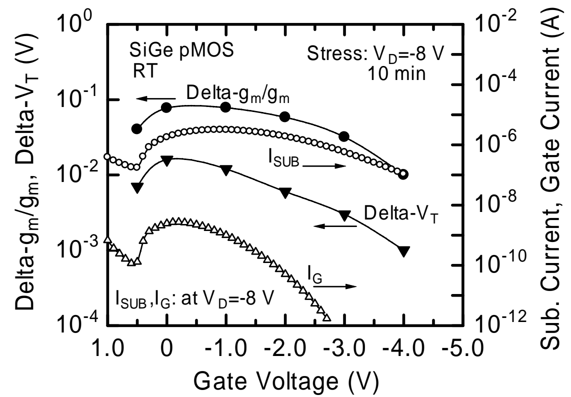

Fig. 2 Degradation of the max. g_m and V_T shift as a function of stress V_G together with corresponding I_{SUB} and I_G for comparison.

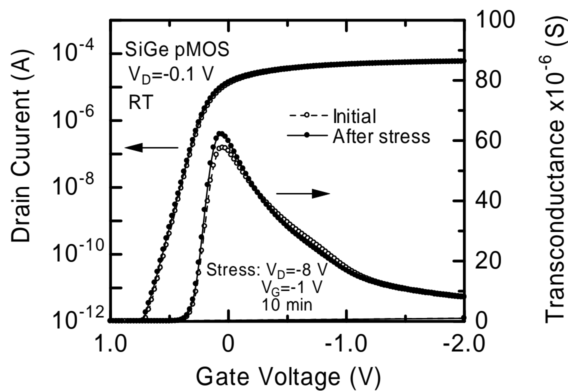

Fig. 1 Drain-current and g_m as a function of V_G before and after hot carrier stress.

In order to identify the cause, low-temperature charge-pumping (LTCP) measurements [6] were performed. The charge pumping (CP) current was measured using a gate pulse of a fixed amplitude (-3 V) and a variable base level between 4 V and 0 V. Examples of the LTCP characteristics at 91 K for various gate-pulse frequencies are shown in Fig. 3, and the dependencies of the two peaks in the CP current in this figure upon the frequency are shown in Fig. 4. Both peaks are proportional to the frequency up to 500 kHz, proving that the CP current is due to interface traps.

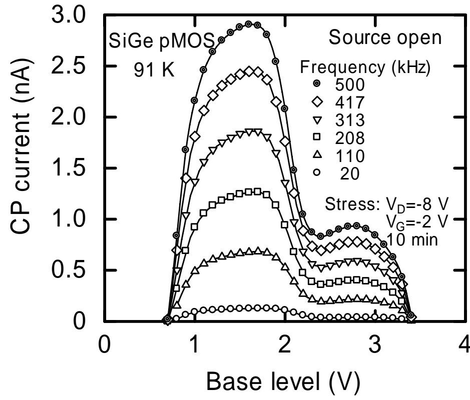

Fig. 3 Low temperature CP characteristics for various gate-pulse frequencies.

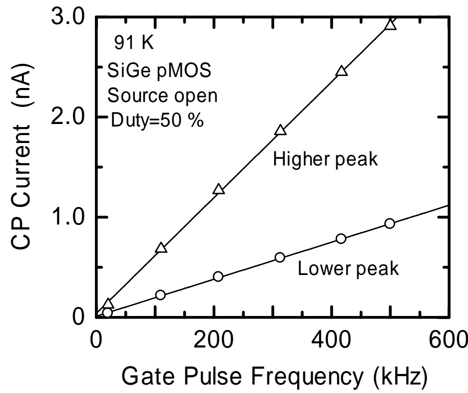

Fig. 4 Values of two peaks in the CP current in Fig. 3 as a function of gate-pulse frequency.

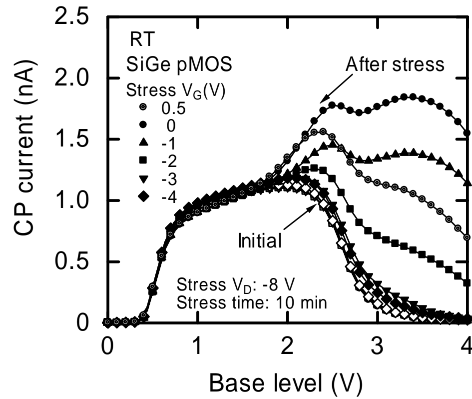

Fig. 5 Stress-V_G dependent CP characteristics at RT.

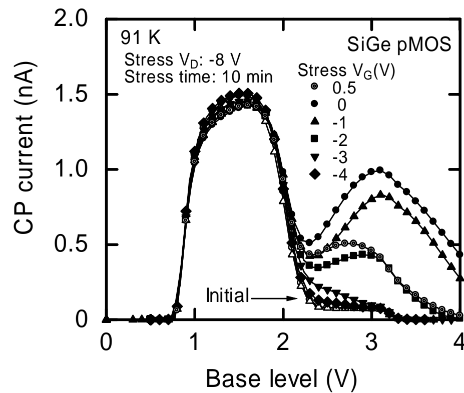

Fig. 6 Stress-V_G dependent CP characteristics at 91 K.

The CP currents observed at base level voltages from 1 to 2 V are mainly due to the gate-oxide interface traps, while those beyond 2.3 V is due to the SiGe/Si hetero-interface traps [3].

Stress-V_G dependent CP characteristics at RT and 91 K are shown in Figs. 5 and 6, respectively, where the frequency of the gate pulse was 250 kHz. From these figures, it is found that the hetero-interface traps are generated after hot-carrier stress, on the other hand, the gate-oxide interface traps are scarcely generated.

Thus, the increase in the maximum g_m and the V_T shift after hot-carrier stress are mainly due to trapped electrons in the gate oxide near the drain, and the decrease in g_m seen over the part of V_G range is considered to be due to generated SiGe/Si hetero-interface traps.

Increase in CP current due to the generated hetero-interface traps is shown in Fig. 7 as a function of stress V_G. I_G and I_{SUB} are also plotted for comparison. The CP current dependence in the figure seems to be

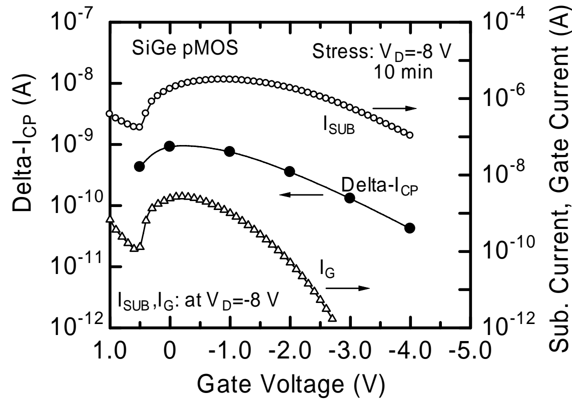

Fig. 7 Increase in CP current due to generated SiGe/Si hetero-interface traps as a function of stress V_G, with changes in I_{SUB} and I_G for comparison.

closer to that of I_G, rather than that of I_{SUB}, which may be explained by considering stress-V_G dependent depth of drain-current path, (i.e., the stress-V_G dependent distance between the hetero-interface and the location of extensive hot-carrier generating), as well as stress-V_G dependent quantity of generated hot-carriers. This subject will be discussed in more detail elsewhere.

4. Conclusions

Degradation of transconductance and threshold-voltage shift after hot-carrier stress in SiGe/Si-hetero-pMOSFETs were discussed based upon the changes in the densities of SiGe/Si hetero-interface and gate-oxide interface traps. These traps were evaluated by a unique low-temperature charge-pumping method. It is concluded that the increase in the maximum transconductance and the threshold-voltage shift after hot-carrier stress are both mainly due to trapped electrons in the gate oxide near the drain, while the decrease in transconductance seen over the part of the gate voltage range is considered to be due to generated SiGe/Si hetero-interface traps.

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