Properties of low-temperature grown InAs and their changes upon annealing

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Abstract

As-grown and annealed samples of InAs layers grown by MBE at 150-350˚C were characterized by electron probe microanalysis (EPMA), high resolution X-ray diffraction (HRXRD), Hall measurements, and secondary ion mass spectrometry (SIMS). EPMA revealed that the As mole fractions in the layers grown at 150-200 ˚C are higher by about 0.5 % than those in the layers grown at 300-350 ˚C. HRXRD measurements revealed that the layers grown at 150-200 ˚C have larger lattice spacings than the InAs substrate by about 0.02 %. Hall measurements revealed that the free-electron concentration in the layer grown at 200 ˚C is as high as 1.4×10^{19} cm^{-3} while such a high concentration of impurities cannot be detected by SIMS. Upon annealing at higher temperatures than 250 ˚C, both the lattice spacing and the free-electron concentration of the layer grown at 200 ˚C were observed to decrease. These phenomena can be reasonably attributed to antisite As.

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Low-temperature (LT) MBE growth has attracted attention since it enables one to grow metastable semiconductor alloys such as MnInAs [1] and TlInAs [2]. It has been already revealed through a large number of studies [3-7] that LT MBE grown GaAs contains a large concentration of antisite As and show very high electrical resistivity upon annealing around 600 ˚C. On the other hand, there is no systematic study on LT MBE grown InAs to date. In this study, InAs layers were grown by MBE on substrates of both GaAs and InAs at 150-350˚C, and were subjected to anneals up to 600 ˚C. Electron probe micro analysis (EPMA), high-resolution X-ray diffraction (HRXRD), Hall measurements, and secondary ion mass spectrometry (SIMS) were used to characterize the layers.

In each growth of the samples, either of a GaAs (001) wafer or an InAs (001) wafer was mounted on Mo substrate holders with In solder. The GaAs wafers used in this study were semi-insulating (S.I.) while the InAs wafers were either of n or p type. Prior to every growth, the substrate temperature was calibrated at the melting point of In by observing the melting of In solder on the Mo substrate holder in the MBE growth chamber. Thermal etching of native oxide on the GaAs or the InAs substrate was performed at 580 or 460 ˚C, respectively, under an As flux. The substrate temperature was then lowered to the growth temperature T_g, which was ranged between 150 and 350 ˚C from sample to sample. An InAs layer was then grown for 30 or 60 min on the substrate. The beam equivalent pressure (BEP) of As was 1×10^{-5} Torr while that of In was set to be 5×10^{-7} Torr which resulted in a growth rate of 1 μm/h. The grown samples were cleaved into several pieces, and some of the pieces were subjected to step-by-step anneals from the growth temperature to 600 ˚C in 50 ˚C increments for 30 min at each temperature in N_2 gas flow.

For the samples grown on InAs substrates, stoichiometry of the as-grown layers was characterized using an electron probe micro analyzer equipped with a wavelength dispersive X-ray spectrometer. The ratio of characteristic X-ray intensities between In and As was measured at three different positions for each sample. The average of the ratios obtained for a sample grown at 350 ˚C was taken as the standard of the stoichiometric InAs. Fig. 1 shows the mole fraction δ of excess As in the $In_{1-\delta}As_{1+\delta}$ grown layers as a function of the growth temperature. Also shown is the mole fraction of excess As in GaAs layers deduced from the data of lattice mismatch in Ref. [7] using the relationship between the lattice mismatch and the antisite As concentration given by Liu et al.[6]. As can be seen in Fig. 1, the excess As concentration in the InAs grown layer increases from about 0.2 % to 0.6 % with decreasing growth temperature T_g from 250 to 200 ˚C, and almost saturates for $T_g \leq 200$ ˚C. This growth-temperature dependence of the excess As concentration in InAs is almost similar to that in GaAs layers.

For the samples grown on InAs substrates, the lattice mismatch of the grown layer to the substrate was characterized using HRXRD. The (004) XRD measurements were performed for the as-grown samples as well as the annealed ones. In the XRD curves of the samples grown at T_g

≥ 250 ˚C, only observed was the sharp symmetric peak due to (004) diffraction from stoichiometric InAs. Annealing up to 400 ˚C caused no change in the XRD curve.

On the other hand, the samples grown at $T_g \leq 200$ ˚C showed an additional peak due to diffraction from the grown InAs layer in the low angle side of the InAs substrate peak in each of their XRD curves. The topmost curve in Fig. 2 shows the (004) XRD curve of the sample grown at 200 ˚C, for an example. Kiessig fringes corresponding to the thickness of the grown layer can be observed around the epi peak. This indicates that the layers grown at $T_g \leq 200$ ˚C have slightly larger lattice spacings than the substrate. Annealing at higher temperatures than 250 ˚C caused marked change in the XRD curves for the samples grown at $T_g \leq 200$ ˚C. As can be seen in Fig. 2, the epi peak was shifted to higher angles across the substrate peak by increasing anneal temperature until 400 ˚C, and then showed gradual shifts toward the substrate peak by further increasing the anneal temperature beyond 400 ˚C. Almost of the other samples grown at $T_g \leq 200$ ˚C showed the similar behavior in their XRD curves upon annealing.

Fitting the XRD curves by the theoretical simulation enabled us to estimate the lattice mismatches of the grown layers against the substrate. The separation angle $\Delta\omega$ of the epi peak from the substrate peak remained to be so small that the epi layers can be assumed to be fully strained without any lattice relaxation. The fitting results are shown by broken curves in Fig. 2. The perpendicular lattice mismatch estimated through the fitting was +0.02% for the as-grown sample while it became –0.04 % after the annealing at 400 ˚C.

As for LT GaAs, it is well known that as-grown layers have larger lattice spacing than stoichiometric GaAs due to the large concentration of antisite As and that the lattice spacing decreases upon annealing [3-5]. It is well established that the decrease in lattice mismatch of LT GaAs upon annealing is due to decrease of antisite As [4, 5]. On the other hand, Wei et al.[3] suggested that the contraction of the LT GaAs to smaller lattice spacing than the GaAs substrate upon annealing at 550-750 ˚C may be associated with lattice vacancies. Bert [4] also reported the lattice contraction of LT GaAs to smaller lattice spacing than the GaAs substrate by annealing at 600 ˚C.

The larger lattice spacing of the as-grown samples of LT InAs can be attributed to the large concentration of excess As. The lattice mismatch against the substrate is not so large in LT InAs as in LT GaAs since the bond length of In-As is not so much smaller as that of Ga-As than the As-As bond length for an antisite defect. Also, decrease in lattice spacing in LT InAs by annealing is probably due to decrease in antisite As concentration as in LT GaAs. The smaller lattice spacing of LT InAs than the InAs substrate caused by annealing above 300 ˚C may be associated with In vacancies. Difference in volume between a vacancy and an In atom at the cation lattice site of InAs will be much larger than that between a vacancy and a Ga atom at the cation lattice site of GaAs. Therefore, the contraction due to vacancies will be more pronounced in InAs than in GaAs.

The vacancies at the cation sites of InAs can be generated through the crystal growing process due to low mobility of In adatoms on the surface at low growth temperatures as well as through the escape of As atoms from the antisites through annealing process.

Hall measurements were performed on the samples grown on S.I. GaAs substrates as well as on those grown on p-type InAs substrates using the Van der Pauw technique. The measurements showed that the grown layers exhibit n-type conduction for all the samples measured. The variable-temperature measurements from room temperature (RT) down to 20K revealed that the free-electron concentration in the as-grown sample grown at 200 ˚C on the S.I. GaAs substrate remains almost constant throughout the temperature range of the measurement. On the other hand, the free-electron concentration remains almost constant from 20K to 200K but shows a steep increase to become ten times around RT in the as-grown samples grown on p-type InAs substrates. This apparent increase in free-electron concentration is thought to be due to conduction in the InAs substrate, as was suggested by Harrison and Houston [8]. The constant free-electron concentrations observed in the low temperature range for the samples grown on the p-type InAs substrates at 200 ˚C and 250 ˚C respectively coincided with those in the samples grown on the S.I. GaAs substrates at the same temperatures. Fig. 3 shows the free-electron concentration as a function of the growth temperature. Crosses indicate the data measured at 80K for the samples grown on p-type InAs substrates while open circles indicate those measured at RT for the samples grown on S.I. GaAs substrates. Also shown by closed circles and squares in Fig. 3 are the free-electron concentration measured at RT for MBE grown InAs on GaAs substrates in Refs. [9] and [10], respectively. One can be see in Fig. 3 the tendency of increase in free-electron concentration with decreasing growth temperature.

Fang et al.[11] revealed by SIMS that carbon is the dominant impurity in InAs grown by organometallic vapor phase epitaxy in the temperature range of 350-600 ˚C, and that its concentration is over two times larger than free-electron concentration. They reported also that the carbon concentration increased with decreasing growth temperature in a similar way to the electron concentration. On the other hand, SIMS measurements in this study revealed that the carbon concentration is below 10^{18} cm^{-3} not only in our sample grown on the InAs substrate at 300 ˚C but also in that grown at 200 ˚C. The large concentrations of free electron over 10^{19} cm^{-3} in our samples grown at 200 ˚C can be attributed to the large concentrations of excess As.

Hall measurements were carried out at RT after every 30-min annealing on the samples grown on GaAs substrates. Fig. 4 shows RT free-electron concentration as a function of annealing temperature. As can be seen Fig. 4, the free-electron concentration decreases drastically with increasing annealing temperature beyond 250 ˚C in the sample grown at 200 ˚C while it does not show so drastic change in both the samples grown at 250 ˚C and 300 ˚C. The annealing temperature dependence of the free-electron concentration in our sample grown at 200 ˚C is very similar to that of the deep donor concentration in a GaAs layer grown at 200 ˚C reported by Look et al.[12]. They identified the deep donor as antisite As. Although antisite As acts as a deep donor in GaAs, it may acts as a shallow donor or a resonant donor in the conduction band in InAs. It is tempting to attribute the annealing temperature dependence of free-electron concentration in the InAs layer grown at 200 ˚C to the decrease in antisite As concentration by annealing.

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Figure captions

Fig. 1 Mole fraction of excess As in InAs (open squares) and in GaAs [7] (closed circles) as a function of growth temperature.

Fig. 2 Change of the XRD curve of an InAs layer grown on an InAs substrate at 200 ˚C due to annealing.

Fig. 3 Free-electron concentration in MBE-grown InAs layers as a function of growth temperature. Crosses indicate the data measured at 80K for InAs grown on p-type InAs substrates in the present study while open circles, closed circles, and closed squares indicate the data measured at RT for InAs grown on GaAs substrates in the present study, Refs. [9] and [10], respectively.

Fig. 4 RT free-electron concentration in InAs grown on GaAs substrates at three different growth temperatures as a function of anneal temperature.